

Compal Confidential

Model Name : CIMS1
File Name : LA-D214P

Compal Confidential

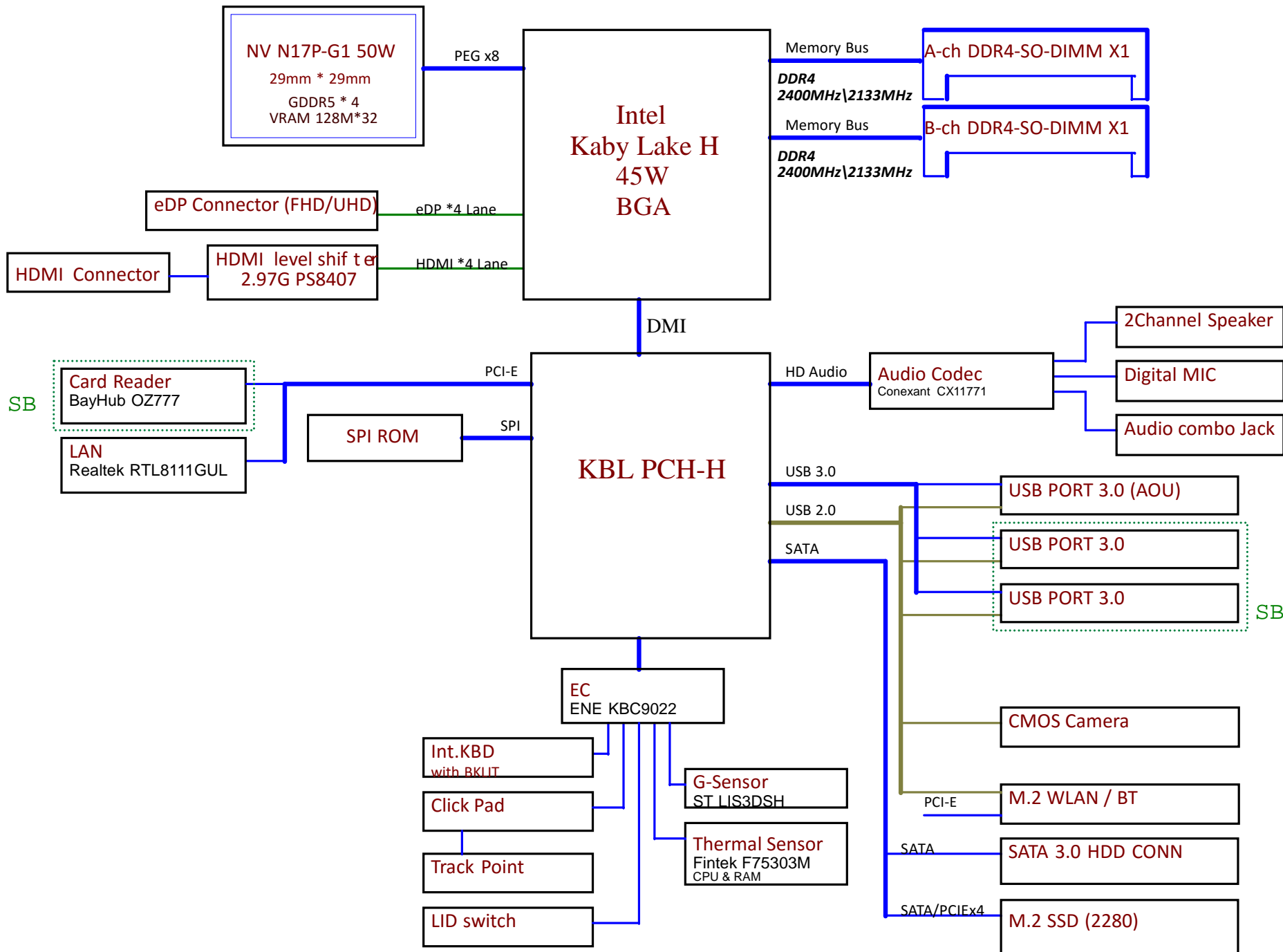
Merlyn M/B Schematics Document

Intel Kaby Lake-H Processor + PCH with DDR4

+ NVIDIA N17P-G1 GPU

Rev. 1.0

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Issued Date	2016/05/13	Deciphered Date	2017/12/31	Title	Cover Sheet
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Voltage Rails

power plane	State	+B	+5VALW +3VALW +1VALW	+1.2V_VDDQ +2.5V +1.0V_VCCST	+1.8VS +5VS +3VS +CPU_CORE +VCCGT +VCCIO +VCC_SA +0.6VS_VTT +1.0VS_VCCSTG +NVVDD +NVVDS +1.8VAON_VGA +1.8VS_VGA +1.0VS_VGA +1.5VS_VGA	
S0		O	O	O	O	
S3		O	O	O	X	
S5 S4/AC		O	O	X	X	
S5 S4/ Battery only		X	X	X	X	
S5 S4/AC & Battery don't exist		X	X	X	X	

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock	
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON	
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF	
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF	
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF	

USB 2.0 Port Table

Port	3 External USB Port	OC# Mapping
1	USB 3.0 Port (SB-Right)	OC0#
2	USB 3.0 Port (SB-Right)	
3		
4		
5	USB 3.0 AOU Port (MB-Left)	OC2#
6		
7		
8	2D Camera	
9		
10		
11		
12		
13		
14	M.2 BT	

USB 3.0 Port Table

Port	
1	USB 3.0 Port (SB-Right)
2	USB 3.0 Port (SB-Right)
3	
4	
5	USB 3.0 Port (MB-Left)
6	
7	
8	
9	
10	

PCIE Port Table

Port	Lane
1	
2	
3	M.2 WLAN
4	LAN
5	
6	
7	
8	
9	M.2 PCIe4
10	
11	
12	
13	Card Reader
14	
15	
16	
17	
18	
19	
20	

SATA Port Table

Port	
0	M.2 SSD
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	

EC SM Bus1 address

Device	Address
Smart Battery	16H
Charger	12H

CPU

UC1	UC1	UC1	UC1	UC1	UC1
ES	ES	QS	QS	i5-R3	i7-R3
KBL-H ES 2.7G QL2X CPU1@ SA0000A1310	KBL-H ES 2.4GQL3X CPU2@ SA0000A1510	KBL-H i5-7300HQ QLM7KBL-H i7-7700HQ QLM5 CPU3@ SA0000AD800	KBL-H i5-7300HQ QLM7KBL-H i7-7700HQ QLM5 CPU4@ SA0000AD700	KBL-H i5-7300HQ QLM7KBL-H i7-7700HQ QLM5 CPU5@ SA0000AD840	KBL-H i5-7300HQ QLM7KBL-H i7-7700HQ QLM5 CPU6@ SA0000AD740

PCH

U2	U2	U2
ES	QS	R3
KBL-H QJGE PCH1@ SA0000B8M60	KBL-H QLF9 PCH2@ SA0000ADB00	KBL-H QLF9 PCH3@ SA0000ADB20

dGPU

U30	U30	U30	U30
ES	QS	PS	R3
N17P-G1 GPU1@ SA0000A0600	N17P-G1 GPU2@ SA0000A0620	N17P-G1 GPU3@ SA0000A0630	N17P-G1 GPU4@ SA0000A0640

VRAM

ZZZ	ZZZ	ZZZ	ZZZ
Hynix	Samsung	Hynix	Samsung
Hynix_2GB X76H2G@ X7664939L21	Samsung_2GB X76H2G@ X7664939L22	Hynix_4GB X76H4G@ X7664939L23	Samsung_4GB X76H4G@ X7664939L24

For EMI BOM

X4E@
X4EA5839L01

BOM Structure Table

BTO Item	BOM Structure	SDV	FVT	SIT	SVT
Connector	ME@	V	V	V	
Unpop	@				
Nvidia GPU	DIS@	V	V	V	
Intel UMA	UMA@	V	V	V	
EMI Un-Mount	@EMI@				
EMI Mount	EMI@	V	V	V	
Hynix 2G VRAM	X76H2G@	V	V	V	
Samsung 2G VRAM	X76S2G@	V	V	V	
Trick Point	TP@	V	V	V	
LAN Switching mode	SWR@	V	V	V	
TPM (LNV UMA Only)	TPM@	V			
N17P-G1	GPU1@	V	V	V	
For EMI BOM	X4E@	V	V	V	
For DGPU HDMI	@HDMI@	V	V		
Nvidia GPU discharge	@DIS@				
ESD requirement	@ESD@				

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

EC SM Bus2 address

Device	Address(7bit)
Thermal Sensor Fintek F75303M	0x9A
Thermal Sensor ON-semi ADM1032	4CH
Nvidia N16P-GT	96H
APS ST LIS3DHTR	30h/31h
CPU Intel SKL-H	

PCH SM Bus address

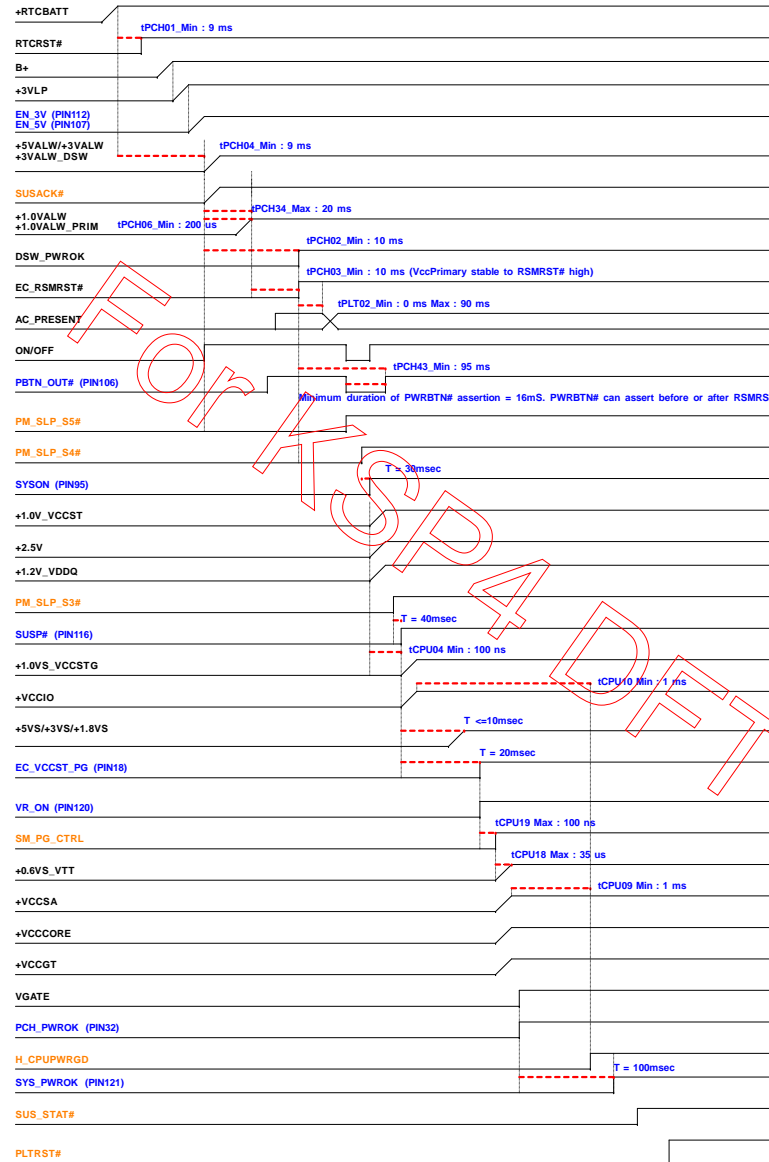
Device	Address(7bit)
DDR DMM1	A0H
DDR DIMM2	A2H
Synaptics Inter Touch Click Pad	2CH

PCB

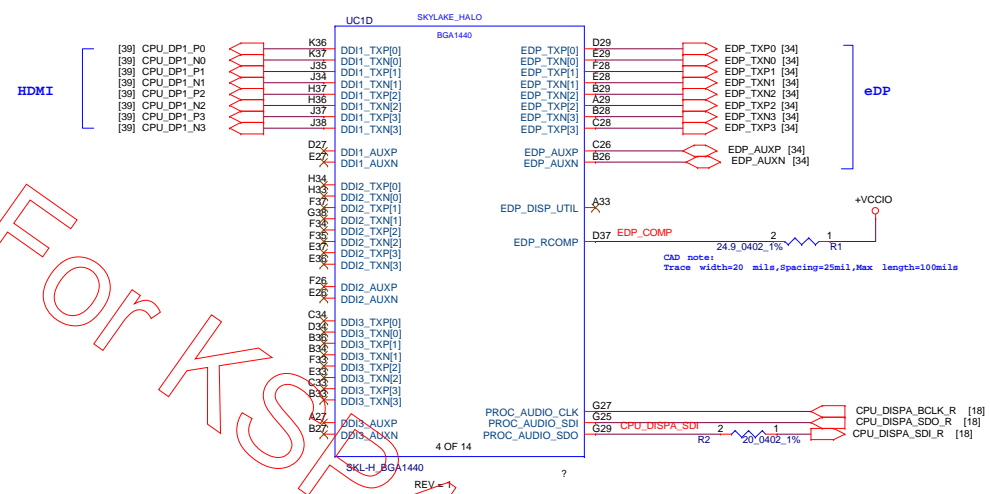
ZZZ
LA-D214P
PCB
DAZ1X500100

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				Notes List
				Size Custom Document Number
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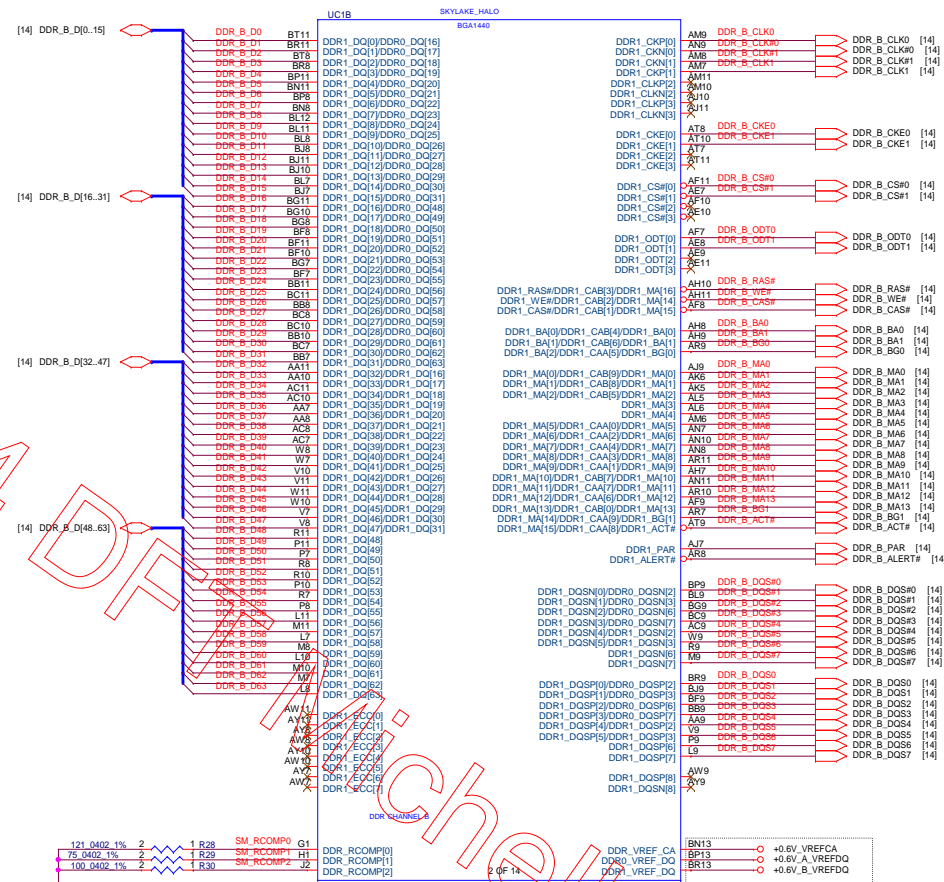
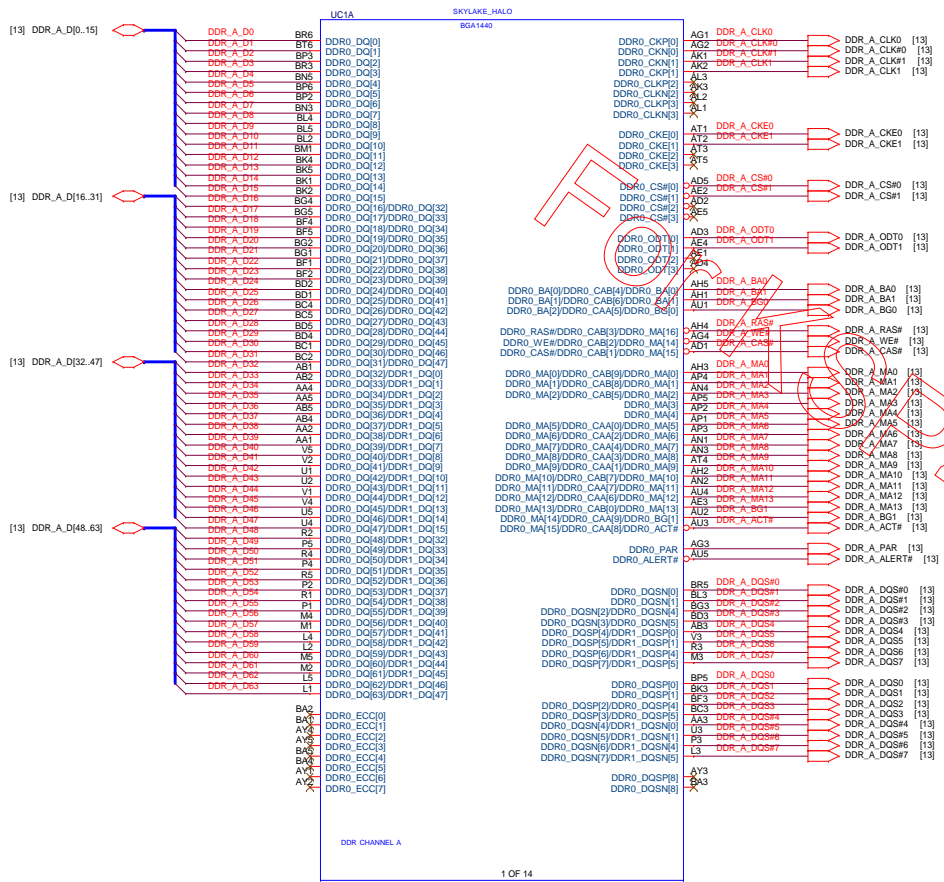
G3->S0



For KSP4 DFT Michelle



Interleaved Memory

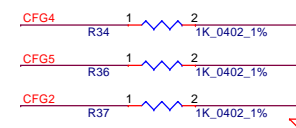
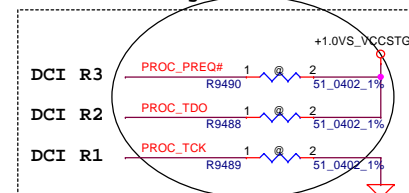


Reference SKL EDS 0.85 Table 6-8
CFG signals internal PH default value = 1

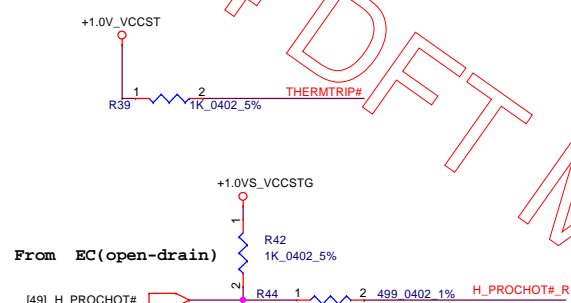
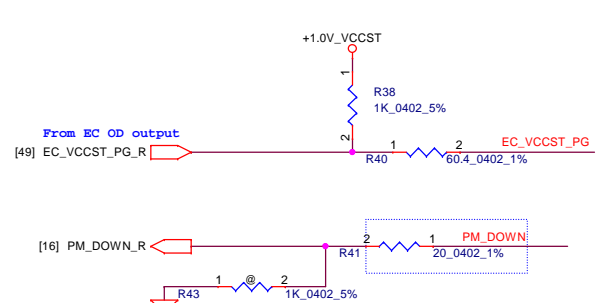
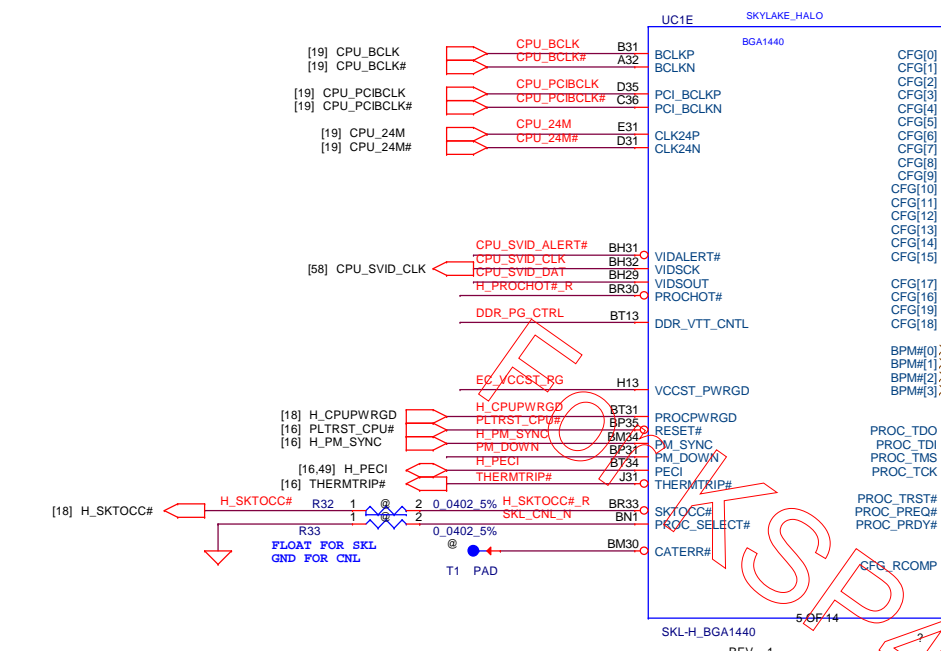
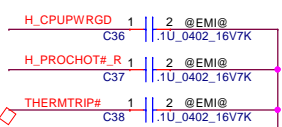
	Description
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted - 1 = (Default) Normal Operation; - 0 = Stall.
CFG[4]	Enable eDP - 1 = Disabled. - 0 = Enabled.
CFG[7]	PEG Training: - 1 = (default) PEG Train immediately following RESET# de assertion. - 0 = PEG Wait for BIOS for training
CFG[1] CFG[3] CFG[8:19]	Reserved configuration lane.

PCIe lane assign	Config. Signals		
	CFG[6]	CFG[5]	CFG[2]
1 x 16	1	1	1
1 x 16 reverse	1	1	0
2 x 8	1	0	1
2 x 8 reverse	1	0	0
1 x 8 + 2 x 4	0	0	1
1x8+2x4 reverse	0	0	0

Intel DCI debug



ESD Reserve ,please close to cpu.
12/30

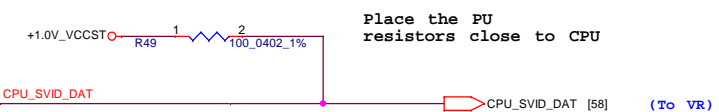


SVID ALERT

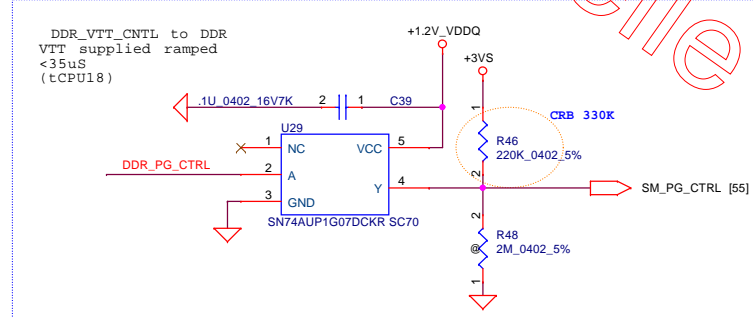


Place the PU resistors close to CPU Follow PDG1.0 Table 12-16

SVID DATA



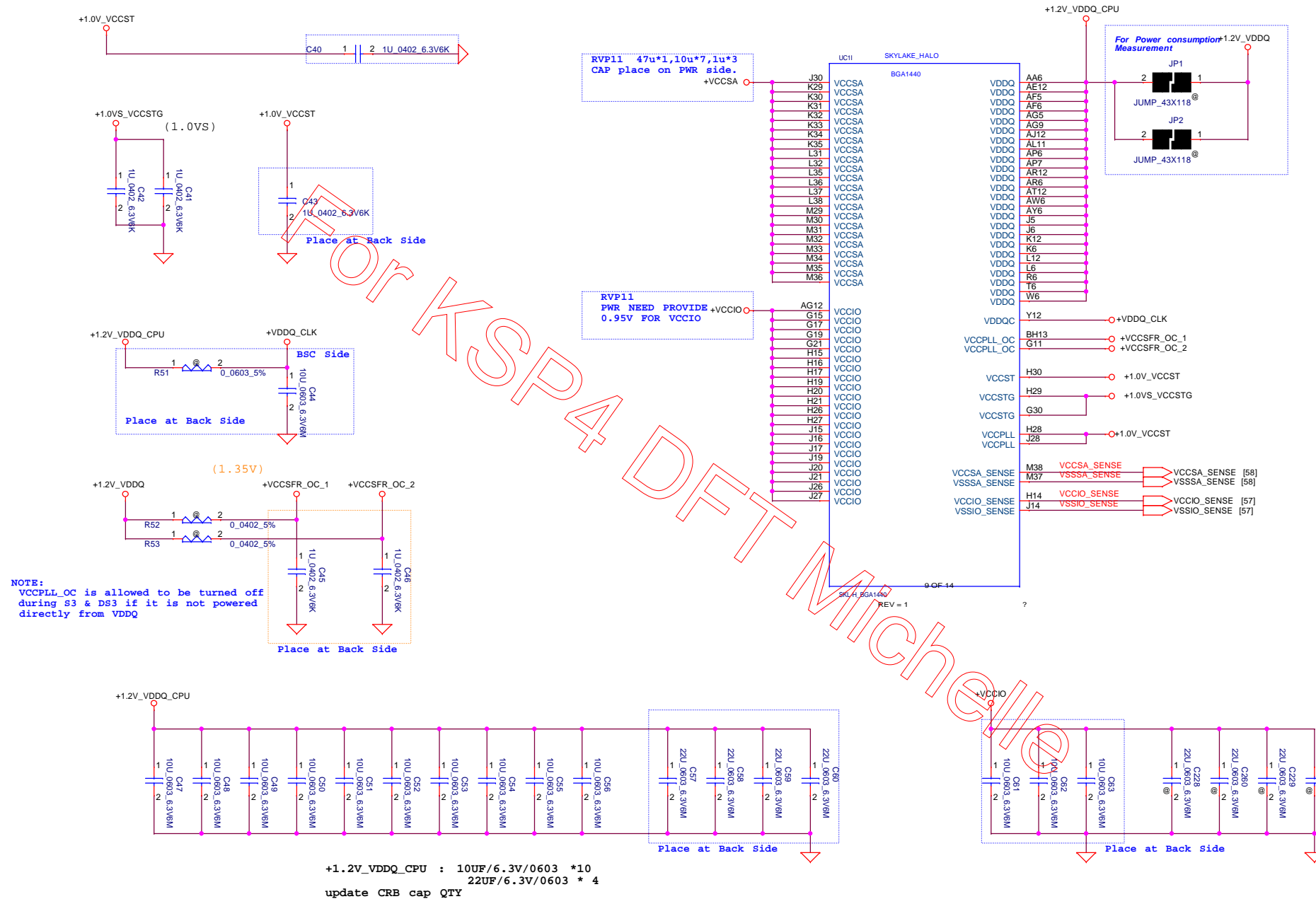
Place the PU resistors close to CPU



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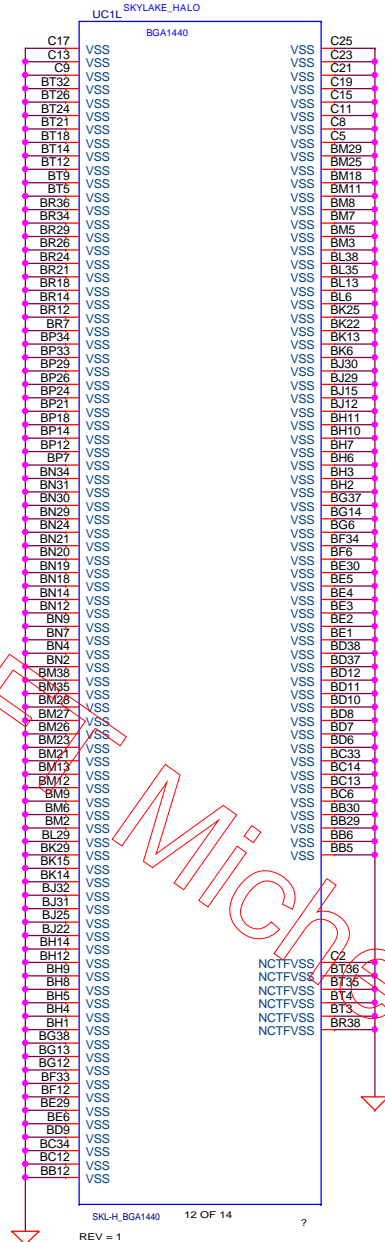
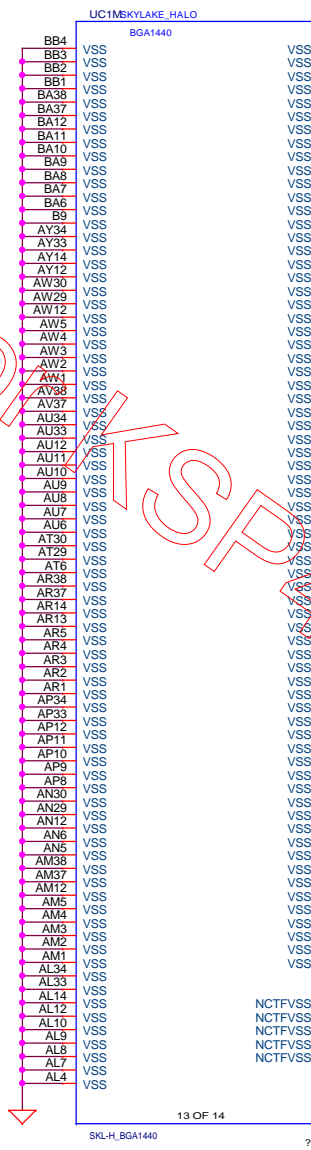
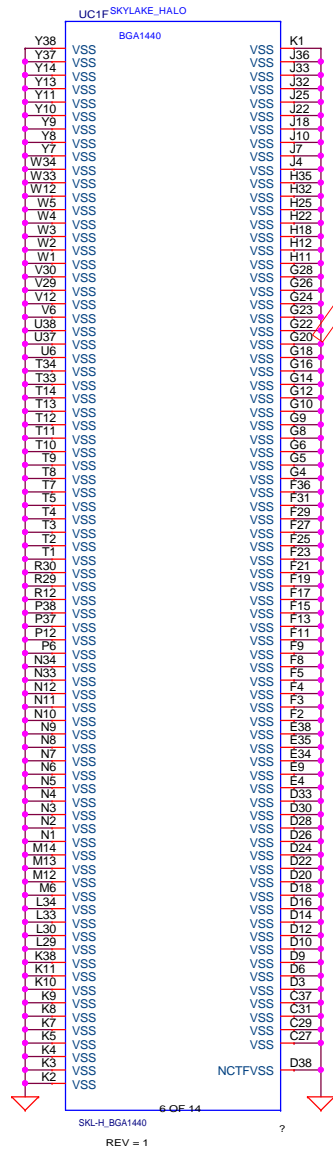
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Title		Compal Electronics, Inc.	
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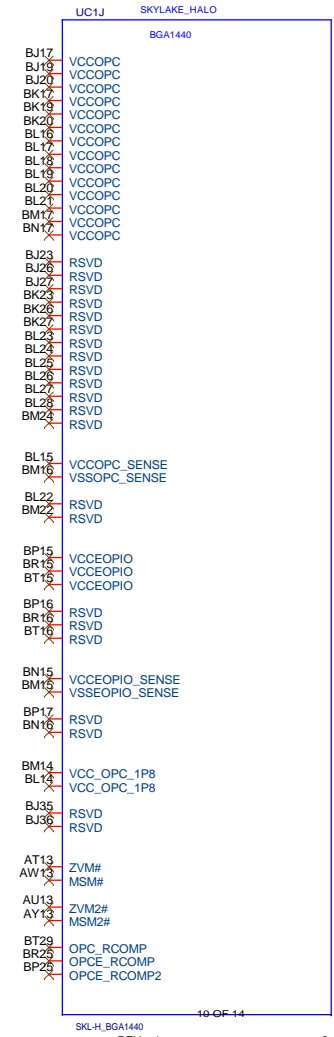
CPU_CORE/VCCGT/VCCSA decoupling capacitor place to PWR side

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EDRAM

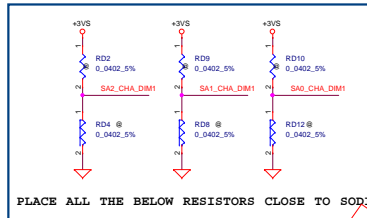
CRB EDRAM



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					Size	Document Number	Rev
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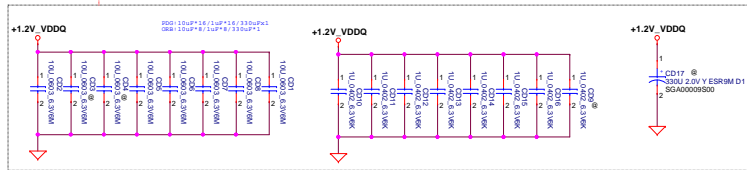
CHANNEL-A Interleaved Memory

Non-ECC DIMM

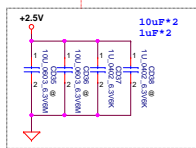


SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

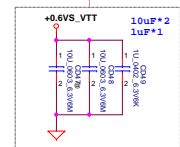
Layout Note:
Place near JDIMM1



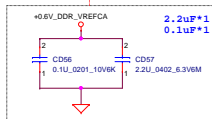
Layout Note:
Place near JDIMM1



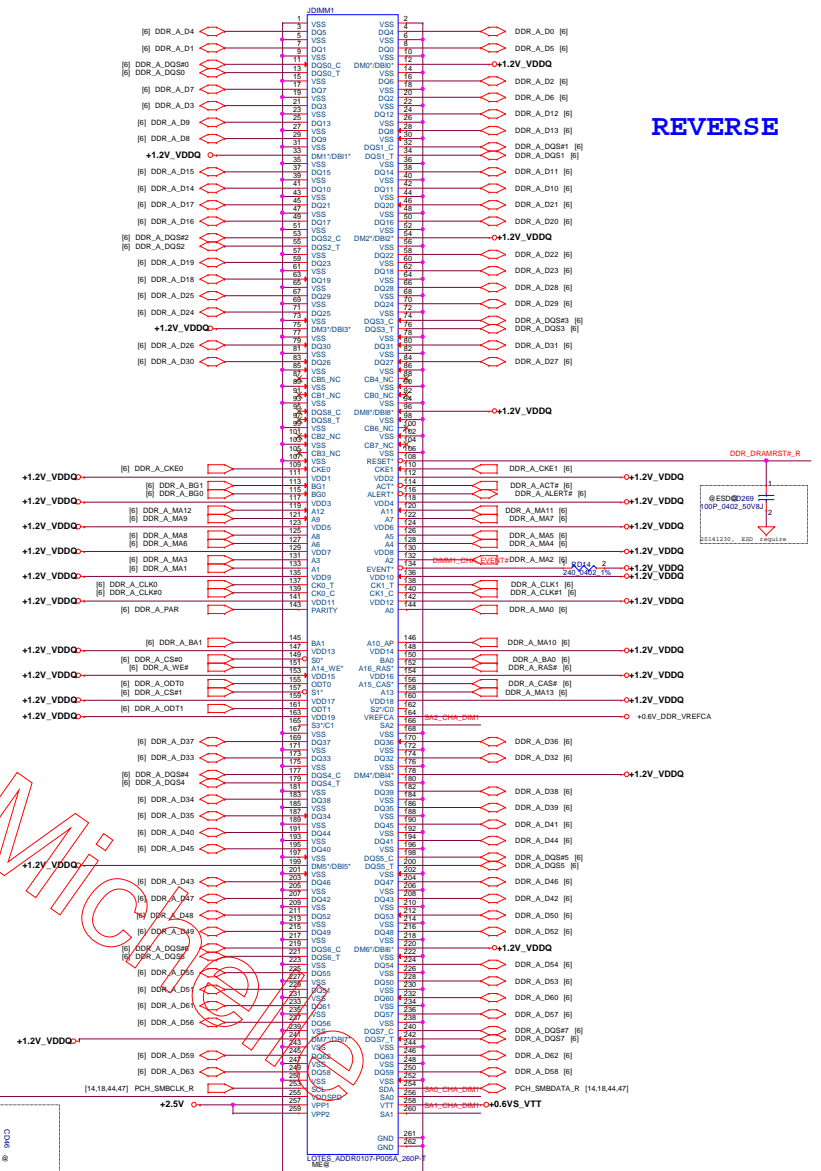
Layout Note:
Place near JDIMM1



Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM1



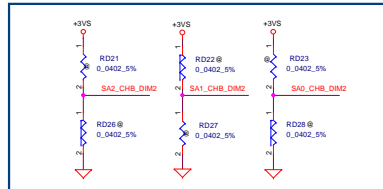
REVERSE



CHANNEL-B

Interleaved Memory

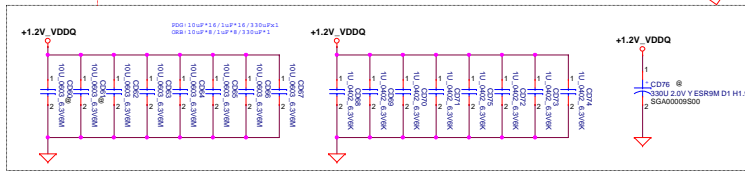
Non-ECC DIMM



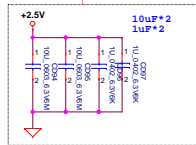
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

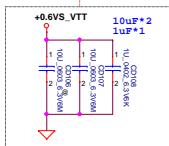
Layout Note:
Place near JDIMM3



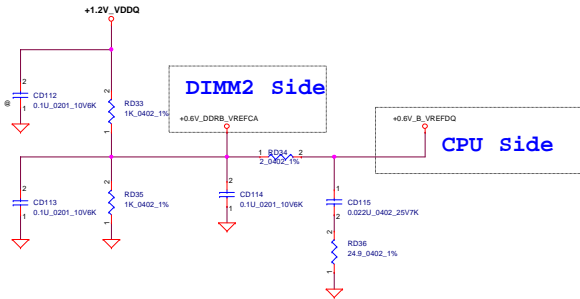
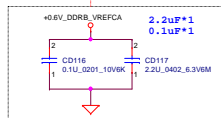
Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2

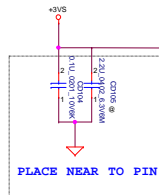


Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2



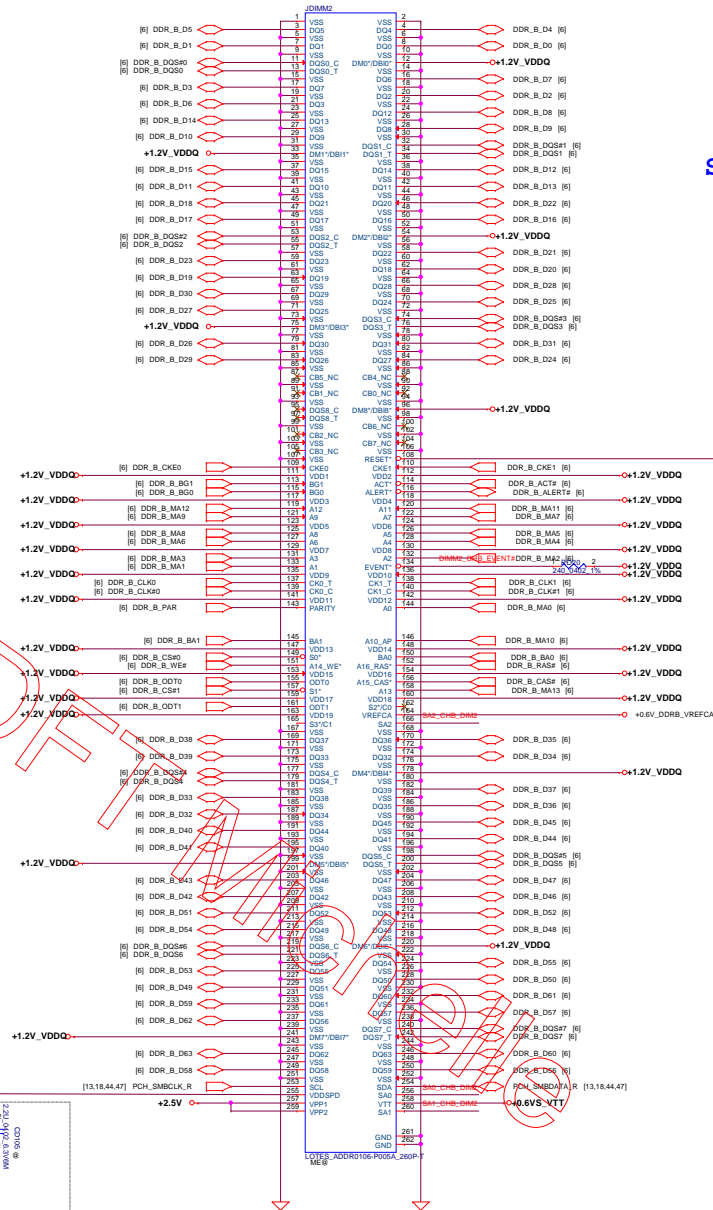
DIMM2 Side

CPU Side

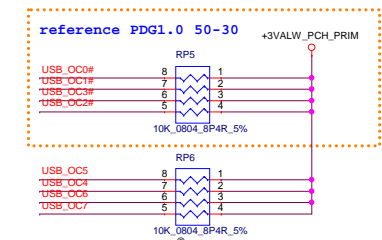
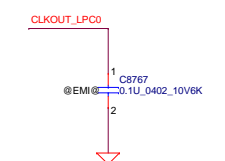
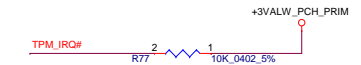
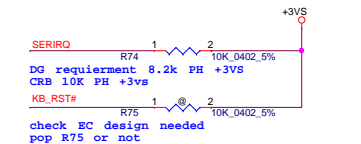
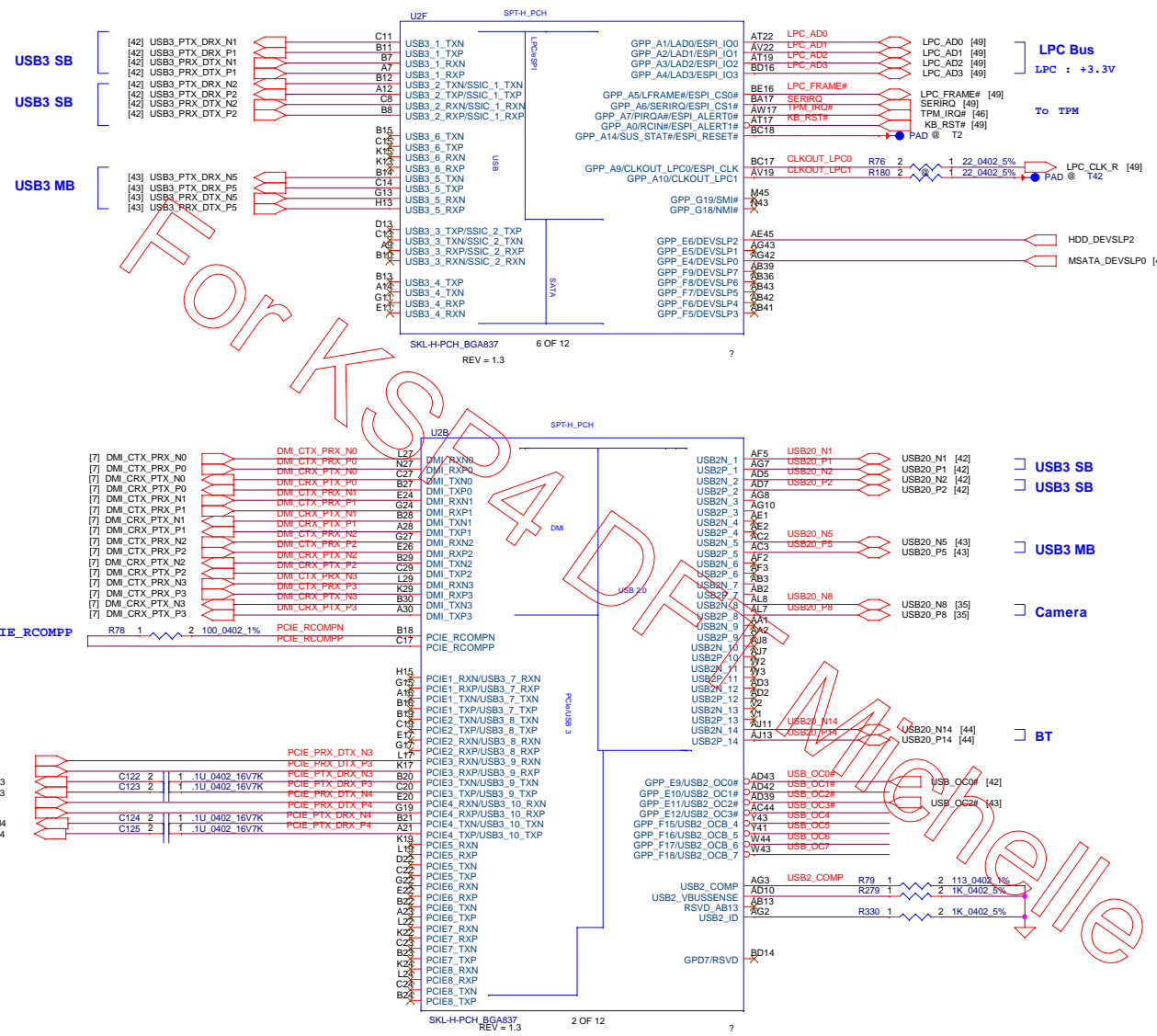


PLACE NEAR TO PIN

STANDARD



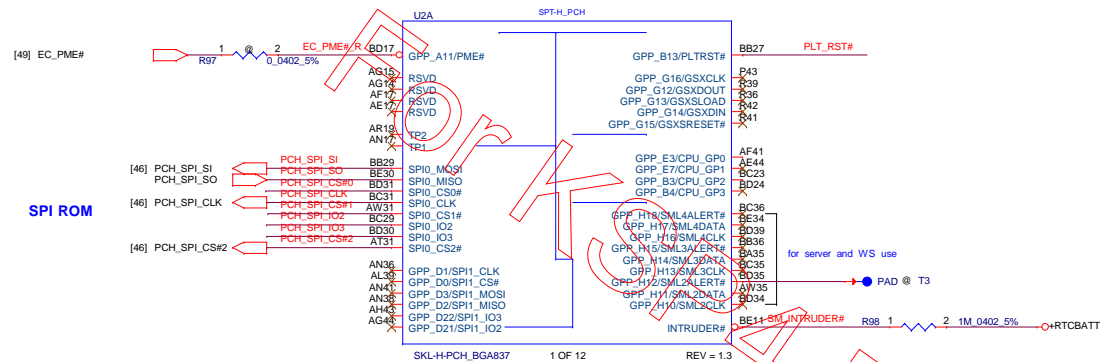
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#543016 P.239 PCIE_RCOMP/PCIE_RCOMP
BO=4 W=12 S=12 R=100ohm

NGFF WL+BT(KEY E)
GLAN

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Functional Strap Definitions

SPI0_MOSI

int. PH

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_MISO

int. PH

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2

int. PH

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3

int. PH

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

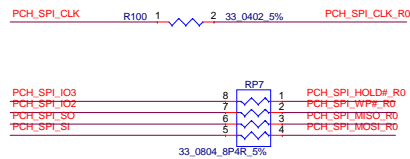
GPP_H12

int. PD

This strap should sample LOW.

SPI Signals

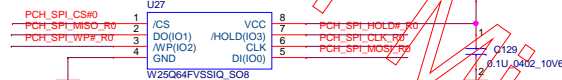
PCH side



ROM side

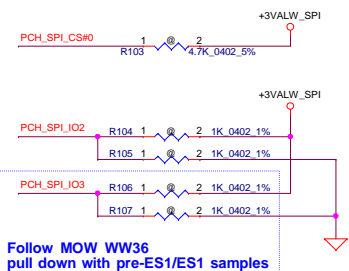
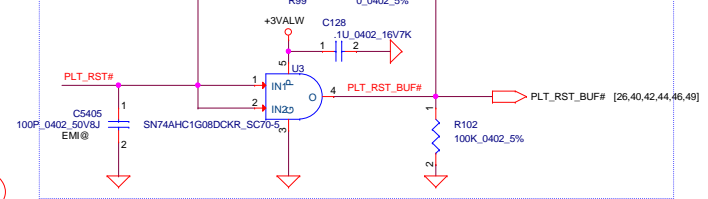
non vPro : 8 M

SPI ROM (8MByte)



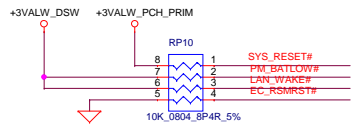
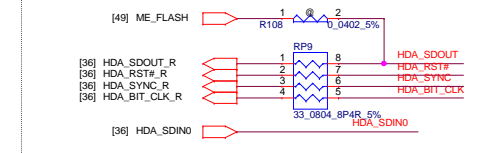
SPI ROM	Vendor	16MB	8MB	4MB
1st	Winbond	SA00005VV10	SA000039A30	SA00003K820
2nd	Micron		SA000099300	

PCH PLTRST Buffer

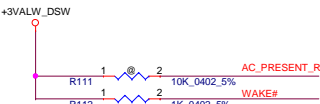


Follow MOW WW36 pull down with pre-ES1/ES1 samples

HDA for AUDIO



Follow 543016_SKL_U_Y_PDG_0_9



WAKE# (DSX wake event)
10 KΩ pull-up to VccIO3
The pull-up is required even if PCIe interface is not used on the platform

EC_RST#

PCH_DPWRK

SYS_PWRK

PCH_DPWRK

SYS_PWRK

PCH_DPWRK

SYS_PWRK

PCH_DPWRK

SYS_PWRK

PCH_DPWRK

SYS_PWRK

PCH_DPWRK

SYS_PWRK

PCH_DPWRK

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PCH_DPWRK

SYS_PWRK

PCH_DPWRK

SYS_PWRK

PCH_DPWRK

SYS_PWRK

PCH_DPWRK

SYS_PWRK

Functional Strap Definitions

SMBALERT# / GPP_C2
int. PD
0 = Disable Intel ME (TLS) (Default) *
1 = Enable Intel ME (TLS)

SML0ALERT# / GPP_C5
int. PD
0 = LPC is selected for EC. (Default) *
1 = eSPI is selected for EC.

SML1ALERT# / PCHHOT# / GPP_B23
int. PD

SPKR / GPP_B14
int. PD
0 = Disable "Top Swap" mode (Default)
1 = Enable "Top Swap" mode.

HDA_SDO
int. PD
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).

DDPB_CTRLDATA / GPP_I6
int. PD
0 = Port B is not detected.
1 = Port B is detected. (Default)

DDPC_CTRLDATA / GPP_I8
int. PD
0 = Port C is not detected.
1 = Port C is detected. (Default)

DDPD_CTRLDATA / GPP_I10
int. PD
0 = Port D is not detected. (Default)
1 = Port D is detected.

HDMI

PCH_DP1_HPD

EC_SCI#_I3

PCH_EDP_HPD

[34] PCH_EDP_HPD

PCH_DP1_HPD

EC_SCI#_I3

PCH_EDP_HPD

[34] PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

PCH_EDP_HPD

EC_SCI#_I3

SPT_H_PCH

GPP_I7/DDPC_CTRLCLK

GPP_I8/DDPC_CTRLCLK

GPP_I9/DDPC_CTRLCLK

GPP_I10/DDPC_CTRLCLK

GPP_I11/DDPC_CTRLCLK

GPP_I12/DDPC_CTRLCLK

GPP_I13/DDPC_CTRLCLK

GPP_I14/DDPC_CTRLCLK

GPP_I15/DDPC_CTRLCLK

GPP_I16/DDPC_CTRLCLK

GPP_I17/DDPC_CTRLCLK

GPP_I18/DDPC_CTRLCLK

GPP_I19/DDPC_CTRLCLK

GPP_I20/DDPC_CTRLCLK

GPP_I21/DDPC_CTRLCLK

GPP_I22/DDPC_CTRLCLK

GPP_I23/DDPC_CTRLCLK

GPP_I24/DDPC_CTRLCLK

GPP_I25/DDPC_CTRLCLK

GPP_I26/DDPC_CTRLCLK

GPP_I27/DDPC_CTRLCLK

GPP_I28/DDPC_CTRLCLK

GPP_I29/DDPC_CTRLCLK

GPP_I30/DDPC_CTRLCLK

GPP_I31/DDPC_CTRLCLK

GPP_I32/DDPC_CTRLCLK

GPP_I33/DDPC_CTRLCLK

GPP_I34/DDPC_CTRLCLK

GPP_I35/DDPC_CTRLCLK

GPP_I36/DDPC_CTRLCLK

GPP_I37/DDPC_CTRLCLK

GPP_I38/DDPC_CTRLCLK

GPP_I39/DDPC_CTRLCLK

GPP_I40/DDPC_CTRLCLK

GPP_I41/DDPC_CTRLCLK

GPP_I42/DDPC_CTRLCLK

GPP_I43/DDPC_CTRLCLK

GPP_I44/DDPC_CTRLCLK

GPP_I45/DDPC_CTRLCLK

SPT_H_PCH

GPP_I7/DDPC_CTRLCLK

GPP_I8/DDPC_CTRLCLK

GPP_I9/DDPC_CTRLCLK

GPP_I10/DDPC_CTRLCLK

GPP_I11/DDPC_CTRLCLK

GPP_I12/DDPC_CTRLCLK

GPP_I13/DDPC_CTRLCLK

GPP_I14/DDPC_CTRLCLK

GPP_I15/DDPC_CTRLCLK

GPP_I16/DDPC_CTRLCLK

GPP_I17/DDPC_CTRLCLK

GPP_I18/DDPC_CTRLCLK

GPP_I19/DDPC_CTRLCLK

GPP_I20/DDPC_CTRLCLK

GPP_I21/DDPC_CTRLCLK

GPP_I22/DDPC_CTRLCLK

GPP_I23/DDPC_CTRLCLK

GPP_I24/DDPC_CTRLCLK

GPP_I25/DDPC_CTRLCLK

GPP_I26/DDPC_CTRLCLK

GPP_I27/DDPC_CTRLCLK

GPP_I28/DDPC_CTRLCLK

GPP_I29/DDPC_CTRLCLK

GPP_I30/DDPC_CTRLCLK

GPP_I31/DDPC_CTRLCLK

GPP_I32/DDPC_CTRLCLK

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GPP_I36/DDPC_CTRLCLK

GPP_I37/DDPC_CTRLCLK

GPP_I38/DDPC_CTRLCLK

GPP_I39/DDPC_CTRLCLK

GPP_I40/DDPC_CTRLCLK

GPP_I41/DDPC_CTRLCLK

GPP_I42/DDPC_CTRLCLK

GPP_I43/DDPC_CTRLCLK

GPP_I44/DDPC_CTRLCLK

GPP_I45/DDPC_CTRLCLK

SPT_H_PCH

GPP_I7/DDPC_CTRLCLK

GPP_I8/DDPC_CTRLCLK

GPP_I9/DDPC_CTRLCLK

GPP_I10/DDPC_CTRLCLK

GPP_I11/DDPC_CTRLCLK

GPP_I12/DDPC_CTRLCLK

GPP_I13/DDPC_CTRLCLK

GPP_I14/DDPC_CTRLCLK

GPP_I15/DDPC_CTRLCLK

GPP_I16/DDPC_CTRLCLK

GPP_I17/DDPC_CTRLCLK

GPP_I18/DDPC_CTRLCLK

GPP_I19/DDPC_CTRLCLK

GPP_I20/DDPC_CTRLCLK

GPP_I21/DDPC_CTRLCLK

GPP_I22/DDPC_CTRLCLK

GPP_I23/DDPC_CTRLCLK

GPP_I24/DDPC_CTRLCLK

GPP_I25/DDPC_CTRLCLK

GPP_I26/DDPC_CTRLCLK

GPP_I27/DDPC_CTRLCLK

GPP_I28/DDPC_CTRLCLK

GPP_I29/DDPC_CTRLCLK

GPP_I30/DDPC_CTRLCLK

GPP_I31/DDPC_CTRLCLK

GPP_I32/DDPC_CTRLCLK

GPP_I33/DDPC_CTRLCLK

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GPP_I39/DDPC_CTRLCLK

GPP_I40/DDPC_CTRLCLK

GPP_I41/DDPC_CTRLCLK

GPP_I42/DDPC_CTRLCLK

GPP_I43/DDPC_CTRLCLK

GPP_I44/DDPC_CTRLCLK

GPP_I45/DDPC_CTRLCLK

SPT_H_PCH

GPP_I7/DDPC_CTRLCLK

GPP_I8/DDPC_CTRLCLK

GPP_I9/DDPC_CTRLCLK

GPP_I10/DDPC_CTRLCLK

GPP_I11/DDPC_CTRLCLK

GPP_I12/DDPC_CTRLCLK

GPP_I13/DDPC_CTRLCLK

GPP_I14/DDPC_CTRLCLK

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GPP_I16/DDPC_CTRLCLK

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GPP_I21/DDPC_CTRLCLK

GPP_I22/DDPC_CTRLCLK

GPP_I23/DDPC_CTRLCLK

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GPP_I25/DDPC_CTRLCLK

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GPP_I27/DDPC_CTRLCLK

GPP_I28/DDPC_CTRLCLK

GPP_I29/DDPC_CTRLCLK

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GPP_I31/DDPC_CTRLCLK

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GPP_I33/DDPC_CTRLCLK

GPP_I34/DDPC_CTRLCLK

GPP_I35/DDPC_CTRLCLK

GPP_I36/DDPC_CTRLCLK

GPP_I37/DDPC_CTRLCLK

GPP_I38/DDPC_CTRLCLK

GPP_I39/DDPC_CTRLCLK

GPP_I40/DDPC_CTRLCLK

GPP_I41/DDPC_CTRLCLK

GPP_I42/DDPC_CTRLCLK

GPP_I43/DDPC_CTRLCLK

GPP_I44/DDPC_CTRLCLK

GPP_I45/DDPC_CTRLCLK

3+VALW_PCH_PRIM

PCH_SMBALERT#

EC_SMB_CK2

EC_SMB_DA2

PCH_SMBCLK

PCH_SMBCLK_R

PCH_SMBCLK

PCH_SMBCLK_R

PCH_SMBCLK

PCH_SMBCLK_R

PCH_SMBCLK

PCH_SMBCLK_R

PCH_SMBCLK

PCH_SMBCLK_R

PCH_SMBCLK

PCH_SMBCLK_R

3+VALW_PCH_PRIM

PCH_SMBALERT#

EC_SMB_CK2

EC_SMB_DA2

PCH_SMBCLK

PCH_SMBCLK_R

PCH_SMBCLK

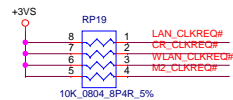
PCH_SMBCLK_R

PCH_SMBCLK

PCH_SMBCLK_R

PCH_SMBCLK

PCH_SMBCLK_R



PH at DGPU side

- [23] PEG_CLKREQ#
- [40] LAN_CLKREQ#
- [44] WLAN_CLKREQ#
- [42] CR_CLKREQ#
- [44] M2_CLKREQ#

- PEG_CLKREQ#
- LAN_CLKREQ#
- WLAN_CLKREQ#
- CR_CLKREQ#
- M2_CLKREQ#

- BC24
- AW24
- AT24
- BD25
- BE25
- AT33
- BD32
- BC32
- BD33
- BC33
- BA33
- AW33
- BD33
- BD33

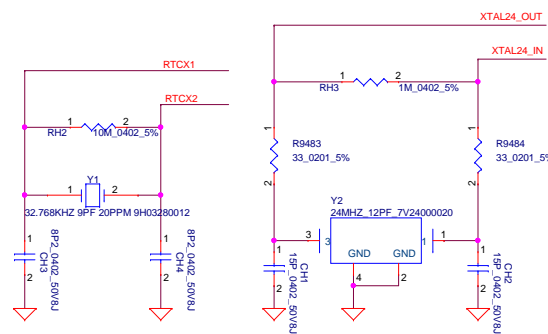
- GPP_B5/SRCCLKREQ0#
- GPP_B6/SRCCLKREQ1#
- GPP_B7/SRCCLKREQ2#
- GPP_B8/SRCCLKREQ3#
- GPP_B9/SRCCLKREQ4#
- GPP_B10/SRCCLKREQ5#
- GPP_H1/SRCCLKREQ6#
- GPP_H2/SRCCLKREQ7#
- GPP_H3/SRCCLKREQ8#
- GPP_H4/SRCCLKREQ9#
- GPP_H5/SRCCLKREQ10#
- GPP_H6/SRCCLKREQ11#
- GPP_H7/SRCCLKREQ12#
- GPP_H8/SRCCLKREQ13#
- GPP_H9/SRCCLKREQ14#
- GPP_H10/SRCCLKREQ15#

- CLKOUT_ITPXD_P
- CLKOUT_ITPXD_N
- CLKOUT_CPUNSSC_P
- CLKOUT_CPUNSSC_N
- CLKOUT_CPUBCLK_P
- CLKOUT_CPUBCLK_N
- CLKOUT_PCIE_N0
- CLKOUT_PCIE_P0
- CLKOUT_PCIE_N1
- CLKOUT_PCIE_P1
- CLKOUT_PCIE_N2
- CLKOUT_PCIE_P2
- CLKOUT_PCIE_N3
- CLKOUT_PCIE_P3
- CLKOUT_PCIE_N4
- CLKOUT_PCIE_P4
- CLKOUT_PCIE_N5
- CLKOUT_PCIE_P5
- CLKOUT_PCIE_N6
- CLKOUT_PCIE_P6
- CLKOUT_PCIE_N7
- CLKOUT_PCIE_P7
- CLKOUT_PCIE_N8
- CLKOUT_PCIE_P8
- CLKOUT_PCIE_N9
- CLKOUT_PCIE_P9
- CLKOUT_PCIE_N10
- CLKOUT_PCIE_P10
- CLKOUT_PCIE_N11
- CLKOUT_PCIE_P11

- CLK_PEG_VGA#
- CLK_PEG_VGA
- CLK_PCIE_LAN#
- CLK_PCIE_LAN
- CLK_PCIE_WLAN#
- CLK_PCIE_WLAN
- CLK_PCIE_CR#
- CLK_PCIE_CR
- CLK_PCIE_M2#
- CLK_PCIE_M2

- CLK_PEG_VGA [23]
- CLK_PEG_VGA [23]
- CLK_PCIE_LAN# [40]
- CLK_PCIE_LAN [40]
- CLK_PCIE_WLAN# [44]
- CLK_PCIE_WLAN [44]
- CLK_PCIE_CR# [42]
- CLK_PCIE_CR [42]
- CLK_PCIE_M2# [44]
- CLK_PCIE_M2 [44]

- dGPU
- GLAN
- NGFF WL+BT (KEY E)
- Card Reader
- M2 SSD

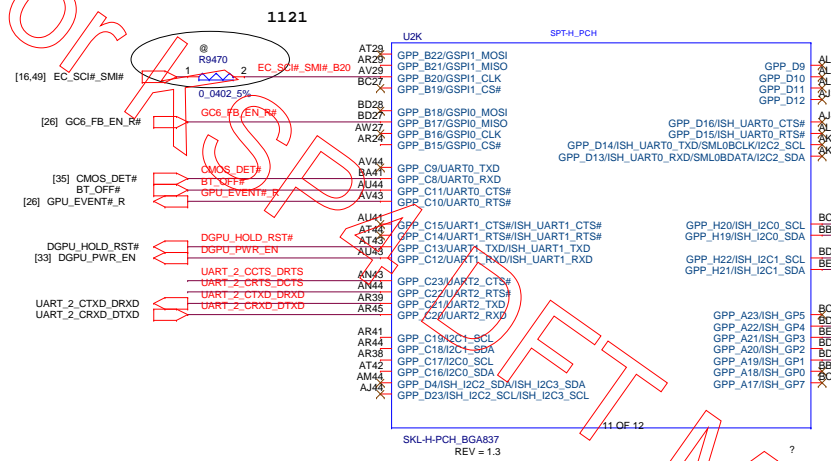
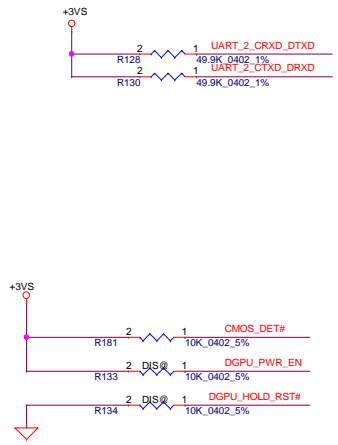


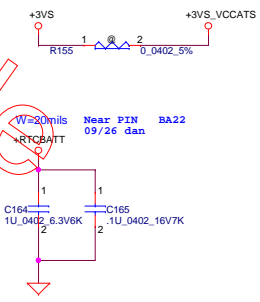
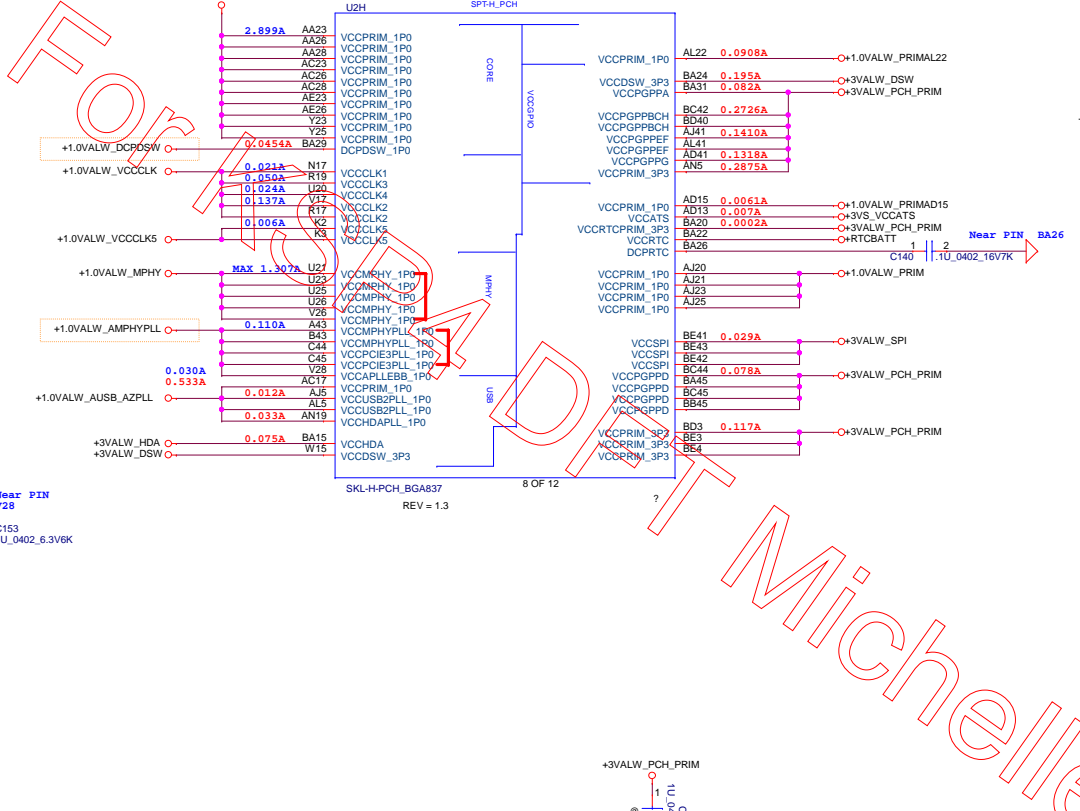
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/05/13	Deciphered Date	2017/12/31	Title	PCH(S/8)CLK
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				Custom	Merlyn2 LA-D214P
				Date:	Monday, November 28, 2016
				Sheet	19 of 66
				Rev	1.0

Functional Strap Definitions

GSP11_MOSI / GPP_B22
int. PD
Boot BIOS Destination
0 = SPI (Default)
1 = LPC

GSP10_MOSI / GPP_B18
int. PD
0 = Disable " No Reboot" mode (Default)
1 = Enable " No Reboot" mode (PCI will disable the TCO
Timer system reboot feature).

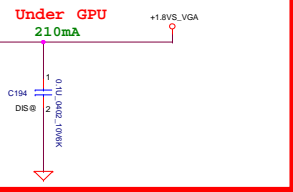




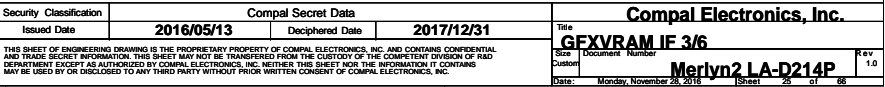
Security Classification	Compal Secret Data			Compal Electronics, Inc. PCH(7/8)POWER		
Issued Date	2016/05/13	Deciphered Date	2017/12/31	Title	PCH(7/8)POWER Merlyn2 LA-D214P	
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				Dustoon		1.0
				Date:	Monday, November 28, 2016	Sheet 21 of 66

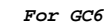
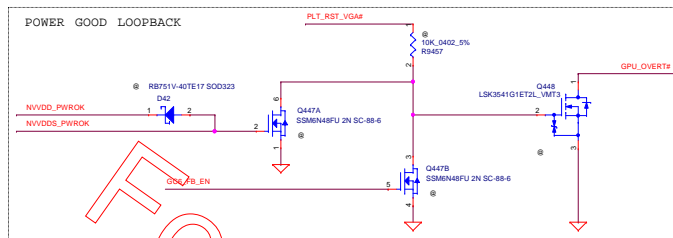
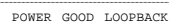


It is a recommendation of NVIDIA to use X6S capacitor arranged in Under and Near GPU.



Security Classification	Compal Secret Data		Title	
Issued Date	2016/05/13	Deciphered Date	2017/12/31	GFX PEG File 1/6
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			Date:	Monday, November 28, 2016 12:21 PM
			Sheet:	1 of 68

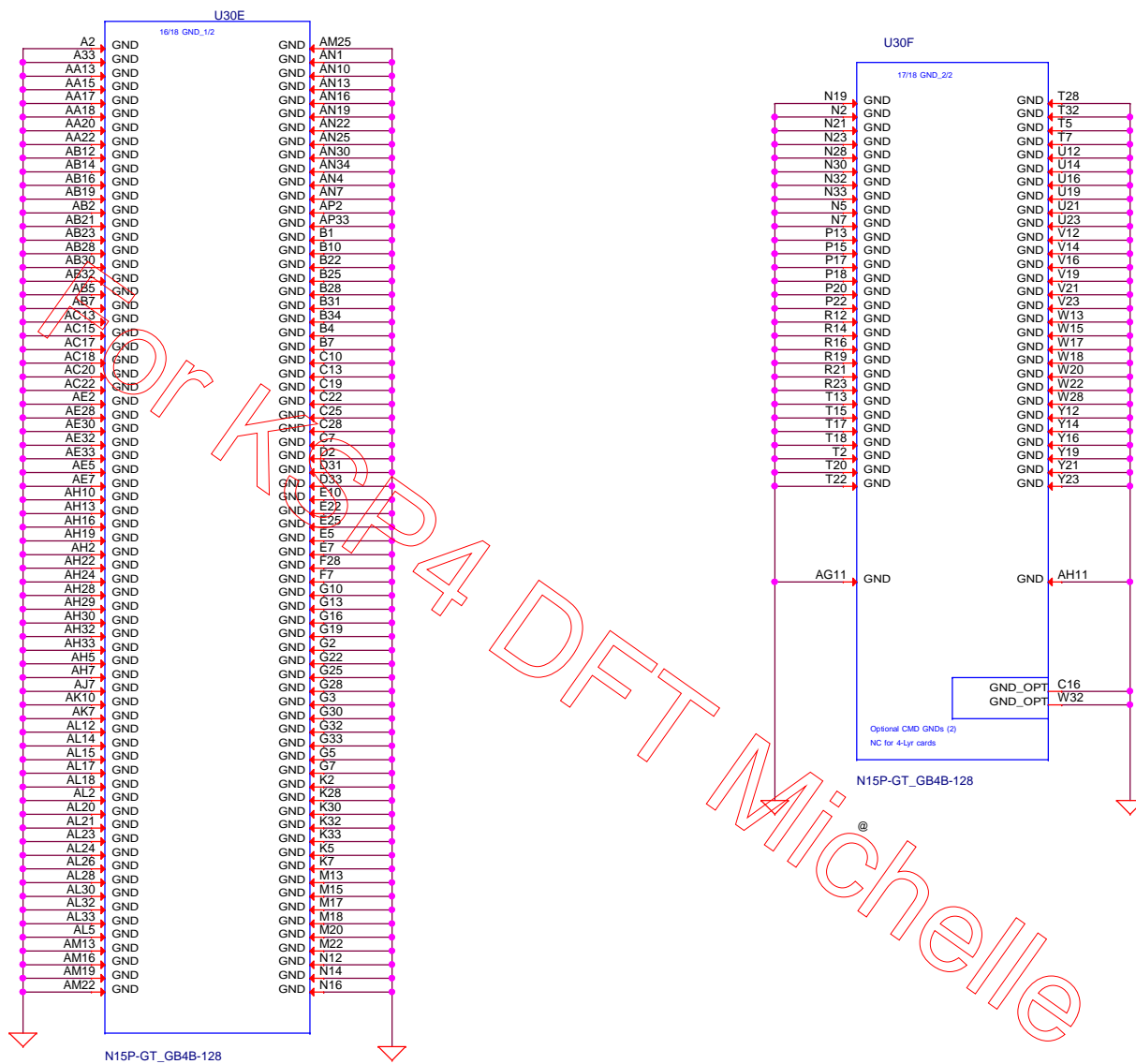




Strap Pins ^{Note 1}			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Row Index	Strap Pins <small>See Note</small>			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
0	H	H	M	disabled	disabled	disabled	disabled

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Issued Date	2016/05/13	Deciphered Date	2017/12/31	File
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			Date: 10/06/2018 11:25:26 AM User: Merilyn2 LG-D214P	
			Date: 10/06/2018 11:25:26 AM User: Merilyn2 LG-D214P	



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2016/05/13	Deciphered Date	2017/12/31	Title	GFX GND 6/6	
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				Merlyn2 LA-D214P		
				Date:	Monday, November 28, 2016	Sheet 28 of 66

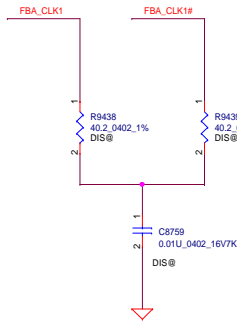
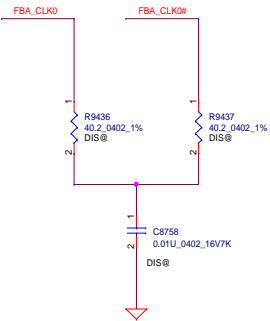


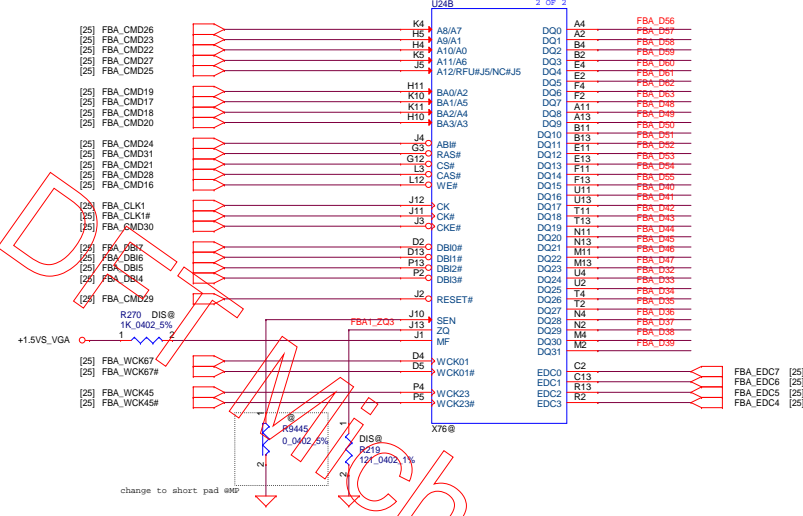
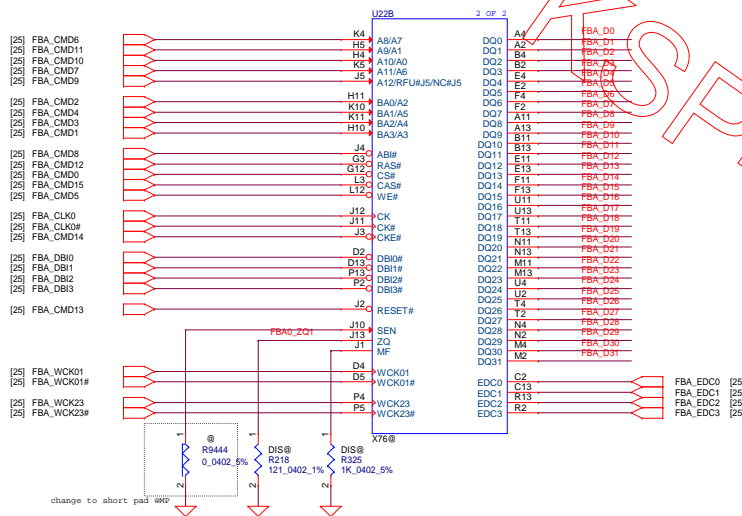
TABLE
GDDR5 VIDEO MEMORY

	HYNIX 256M x16	SAMSUNG 256M x16
U22 U24 U26 U28	H5GC4H24MFR-T2C	K4G41325FE-HC28

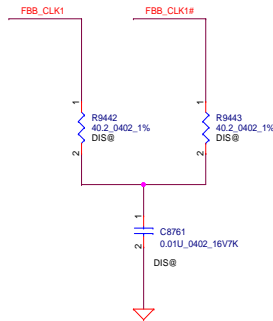
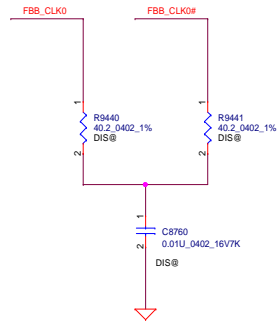
FB CMD mapping Mode H -N16x GDDR5

MF=0

MF=1



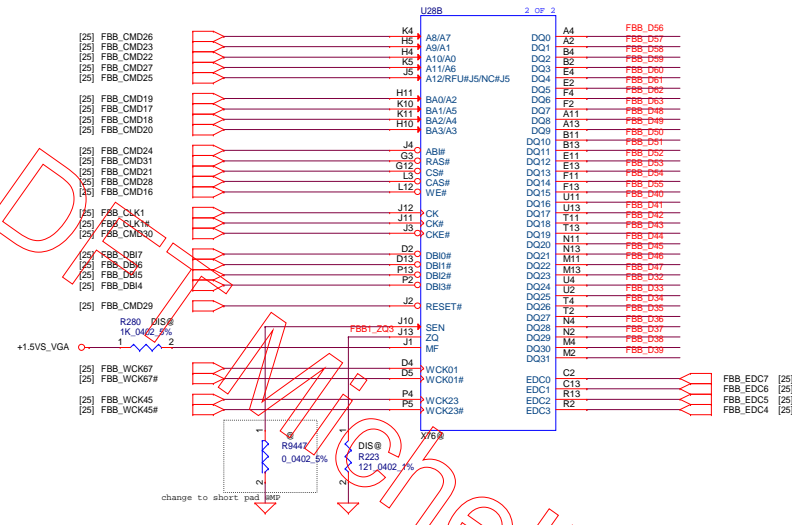
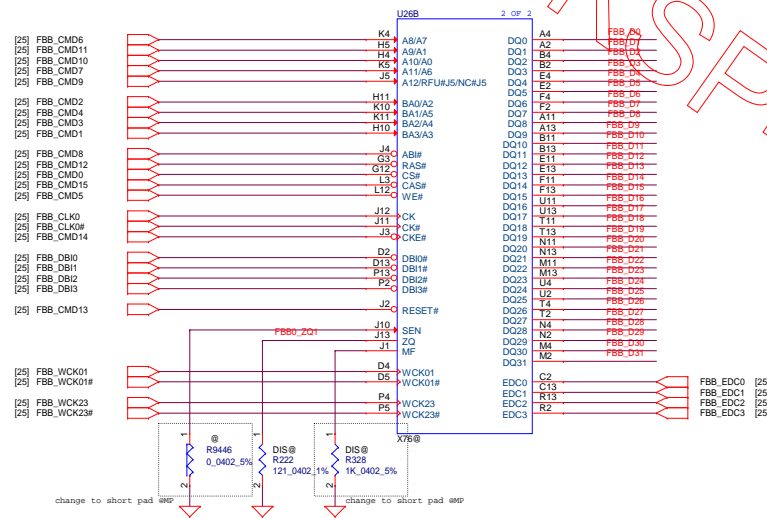
GDDR5 VRAM Mirror Mapping table											
BYTE0		BYTE1		BYTE2		BYTE3		Address		Control	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24	DQ8	DQ16	DQ16	DQ8	DQ24	DQ0	A8/A7	A10/A0	RAS#	CAS#
DQ1	DQ25	DQ9	DQ17	DQ17	DQ9	DQ25	DQ1	A9/A1	A11/A6	CS#	WE#
DQ2	DQ26	DQ10	DQ18	DQ18	DQ10	DQ26	DQ2	A10/A0	A8/A7	CAS#	RAS#
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DQ4	DQ28	DQ12	DQ20	DQ20	DQ12	DQ28	DQ4	BA0/A2	BA2/A4	WCK01#	WCK23#
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DQ6	DQ30	DQ14	DQ22	DQ22	DQ14	DQ30	DQ6	BA2/A4	BA0/A2	WCK23#	WCK01#
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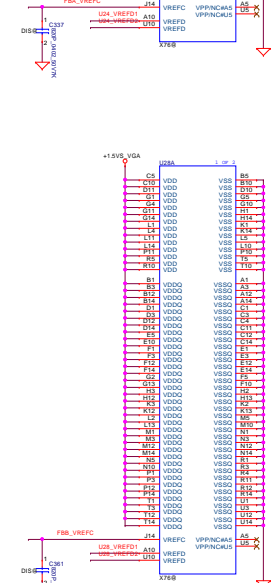
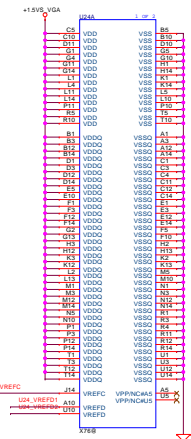
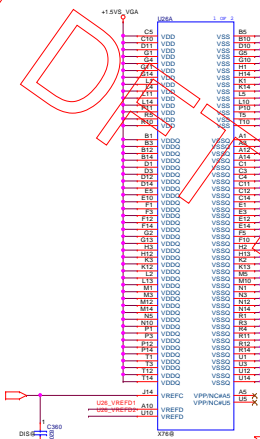
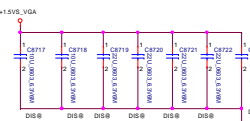
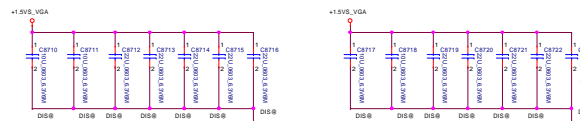
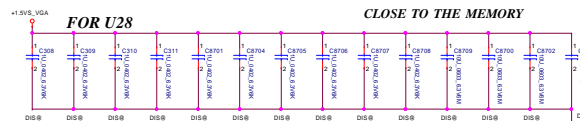
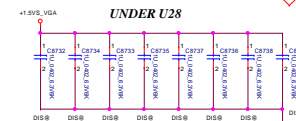
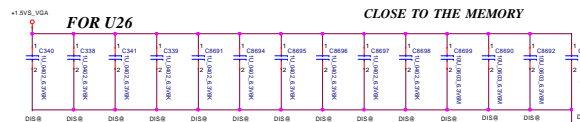
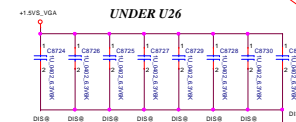
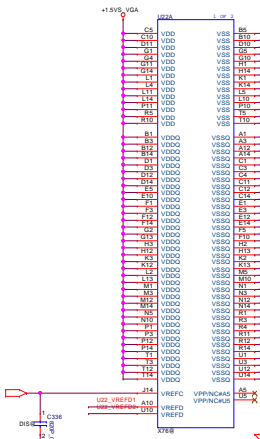
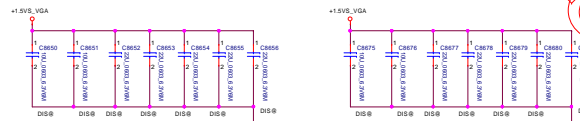
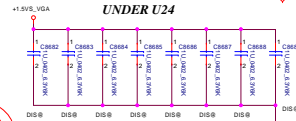
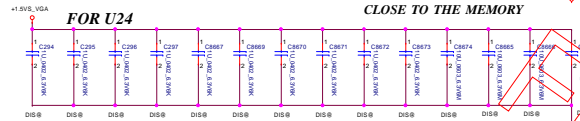
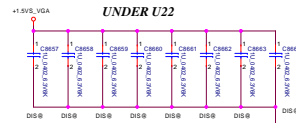
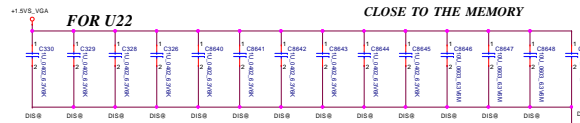


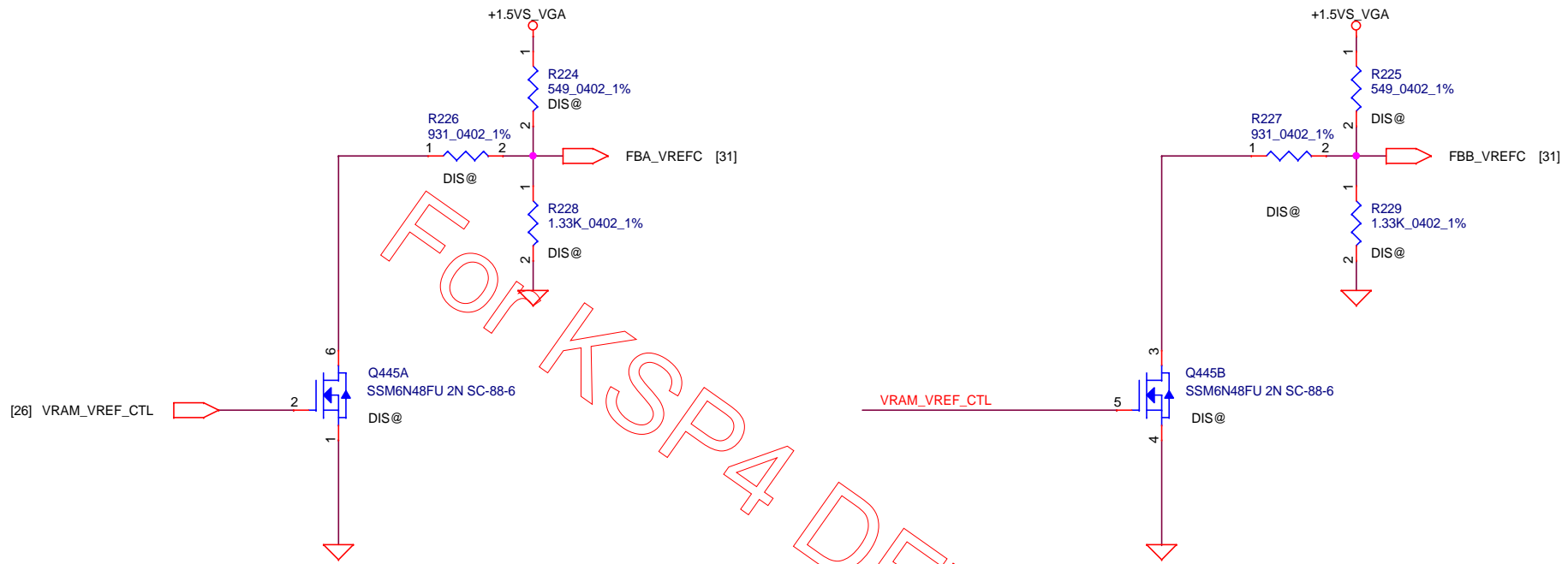
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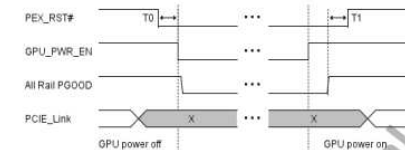
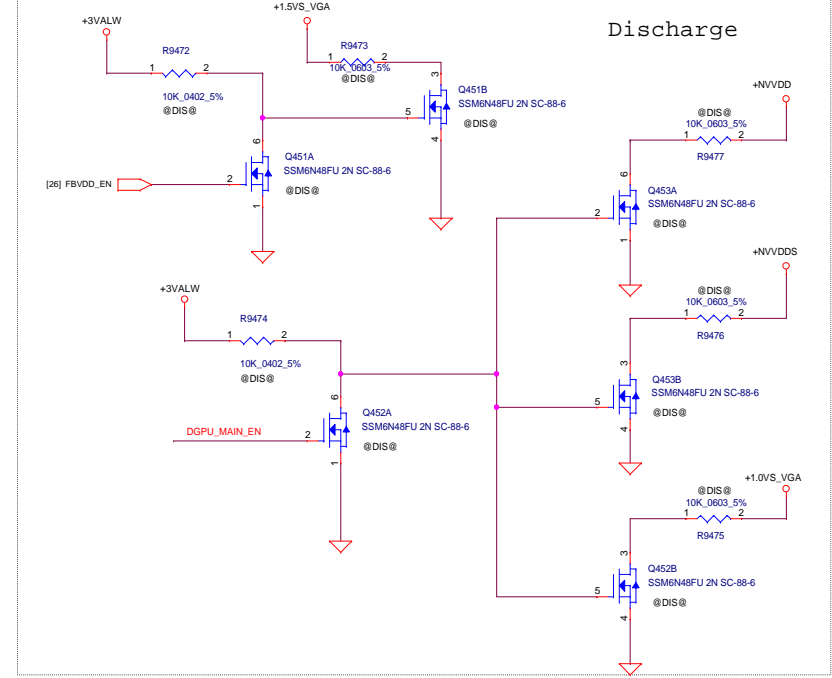
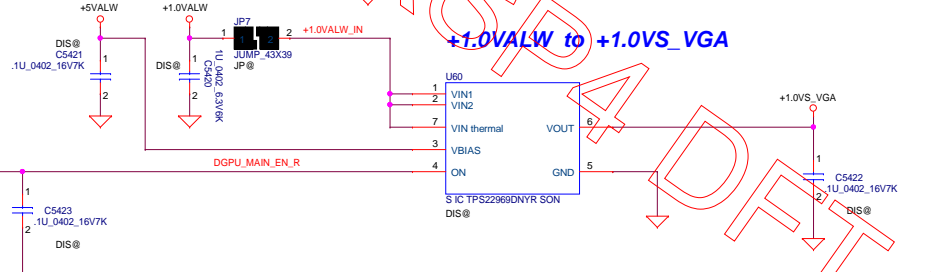
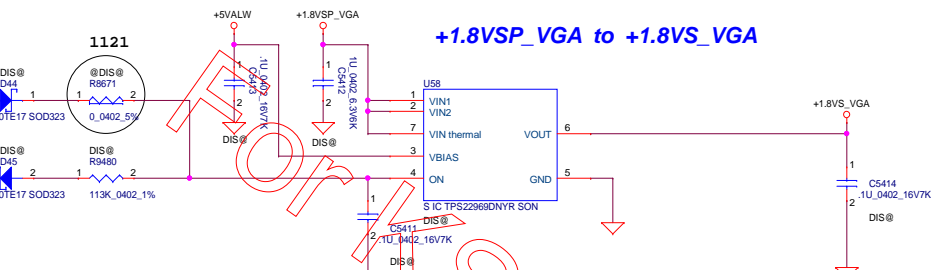
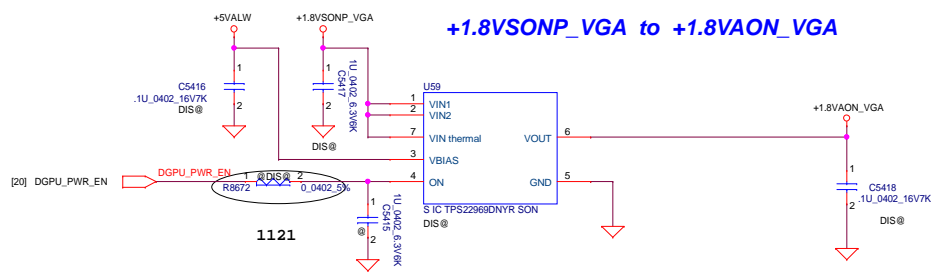
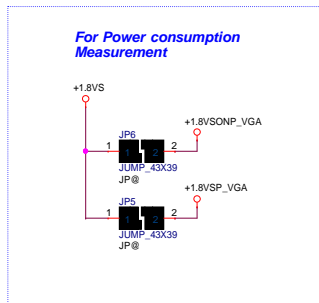


Figure 8.7 Optimus Entry/Exit Timing Diagram

Table 8.1 Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

7.3.2.1 Power-Up Sequence

The following power-up sequence is required:

1V8_AON → 1V8_MAIN → NVVDD → NVVDDS / PEX_DVDD → FBVDD(Q)

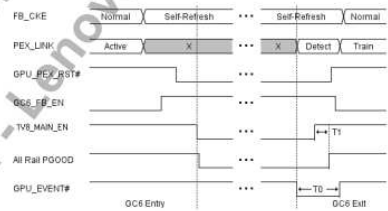
- ▶ All GPU power rails must ramp up after 1V8_AON.
- ▶ FBVDD(Q) should ramp up after NVVDDS and PEX_DVDD.

7.3.2.2 Power-Down Sequence

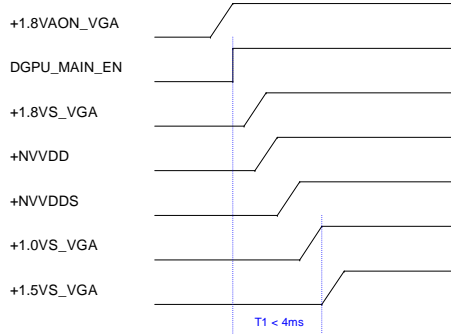
The following power-down sequence is required:

- ▶ NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD;

Figure 8.15 GC6 2.1 Entry/Exit Sequence Timing Diagram



GPU Power Up Sequence



The ramp time for any rail must be more than 40us and less than 2ms.

GPU Power Down Sequence

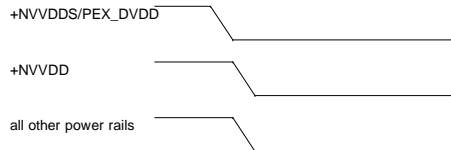
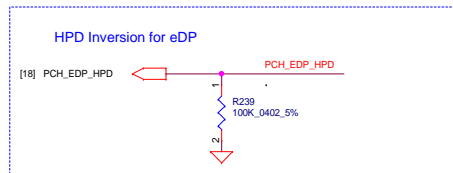
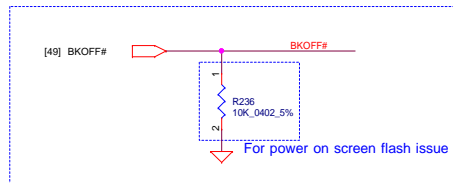


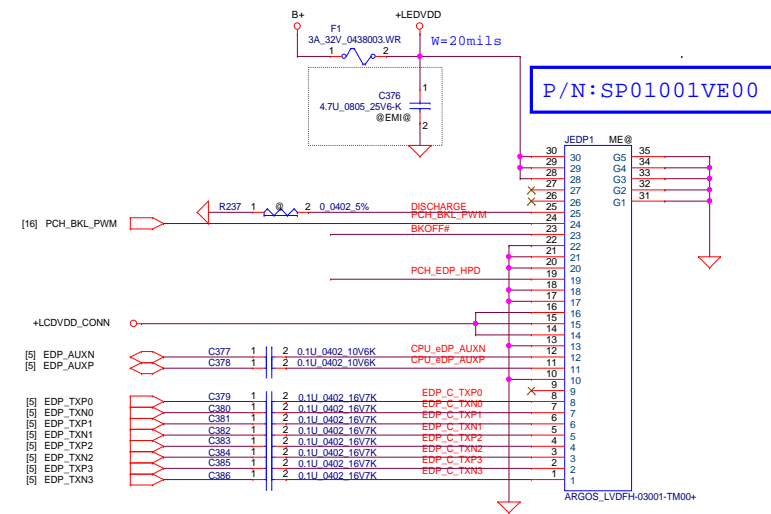
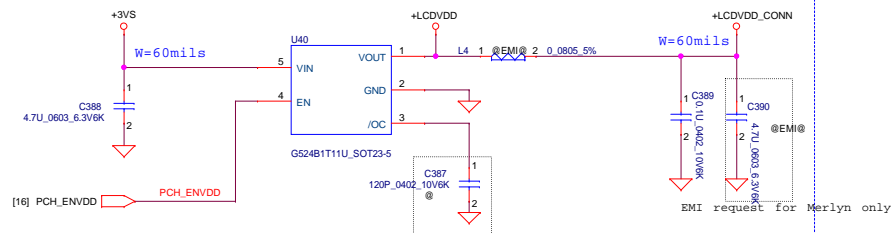
Table 8.2 GC6 2.1 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

eDP Panel Conn



LCD POWER CIRCUIT



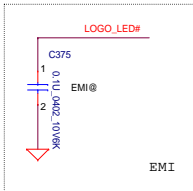
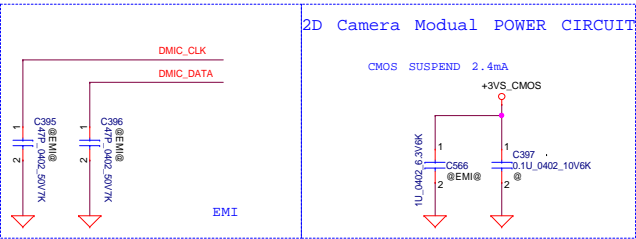
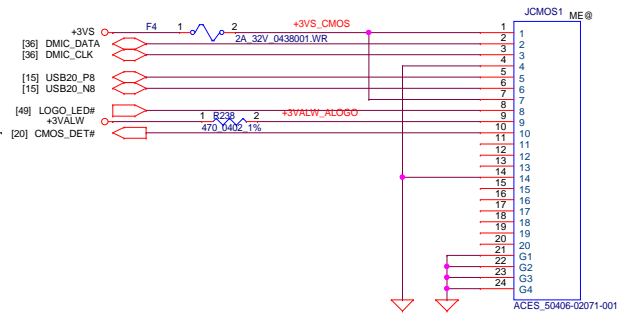
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2D Camera

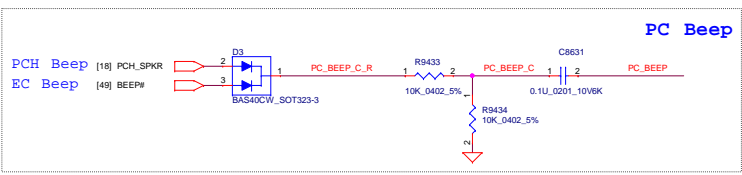
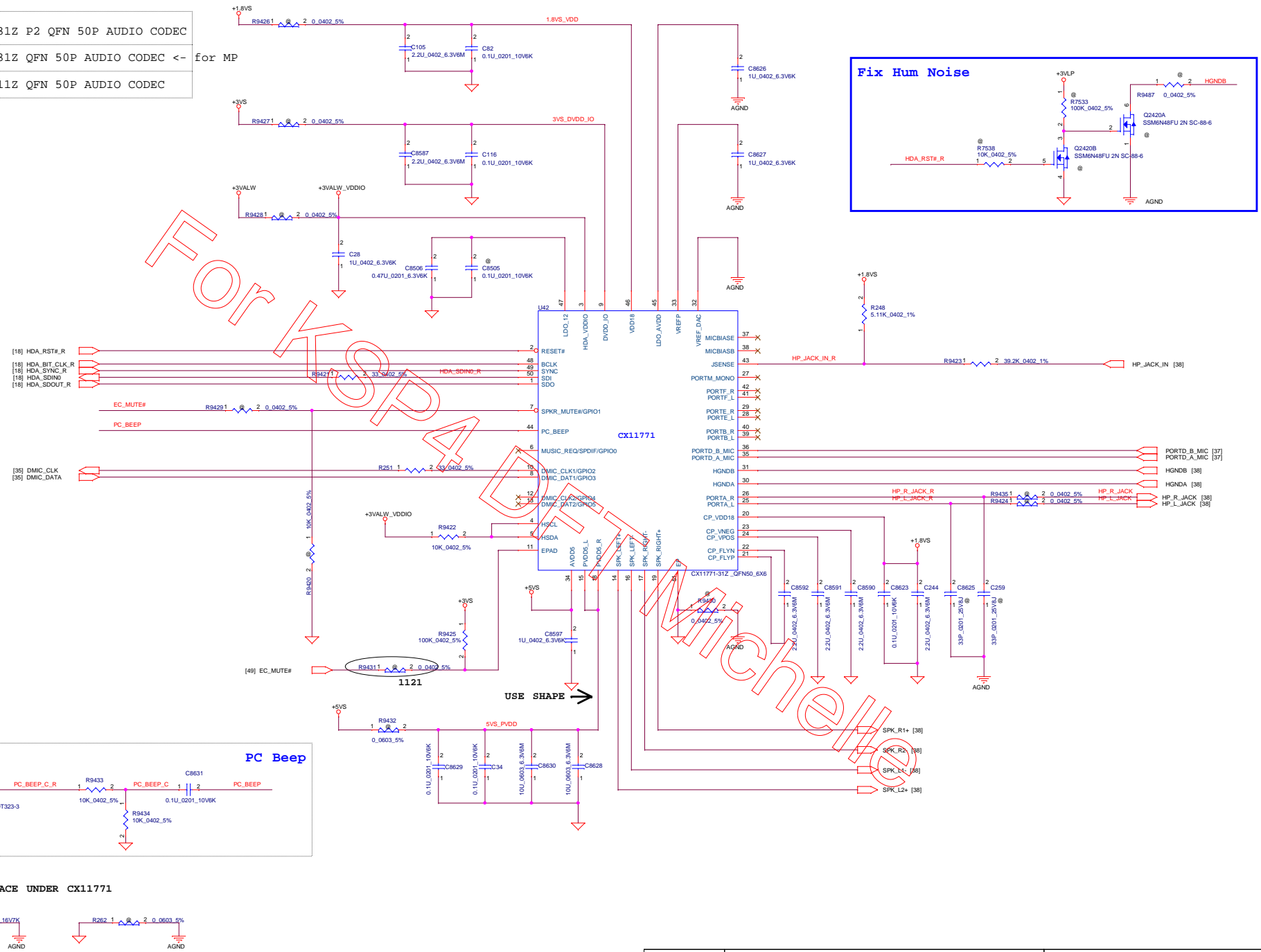
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CMOS_DET#	NC	2D_Camera
	High	LOW
This pin is used for define the SKU of system. Because the pin define are not same in both systems.		

DMIC
2D CMOS
A LOGO RED LIGHT



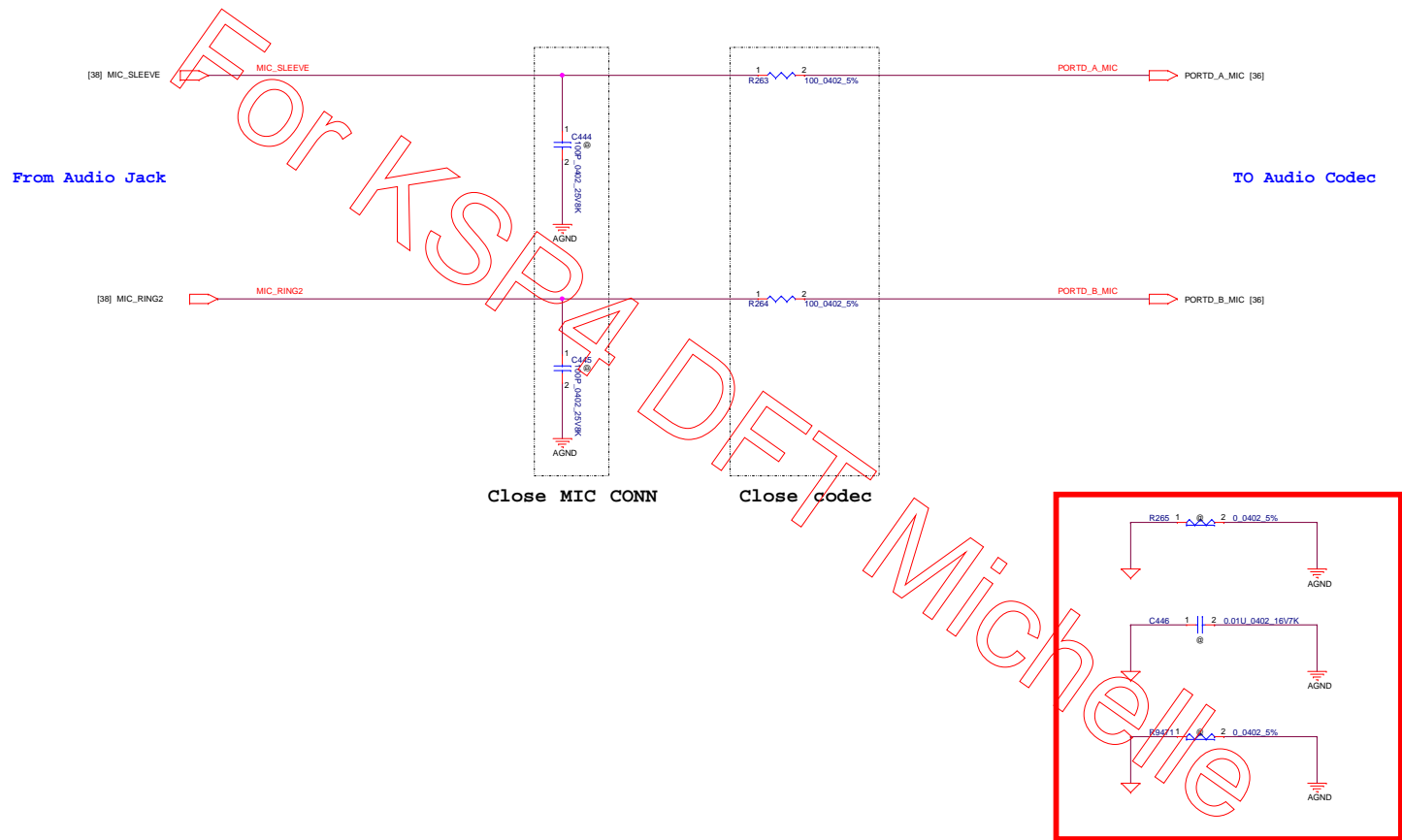
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PLACE UNDER CX11771



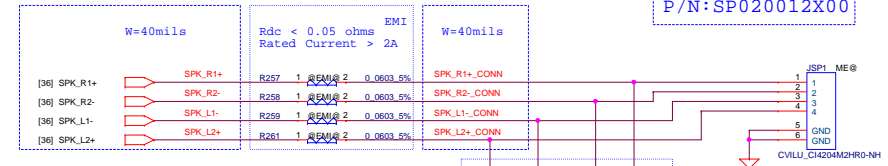
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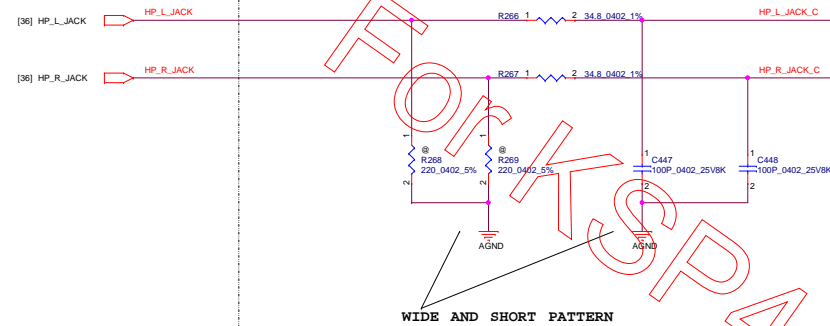
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Internal Speaker

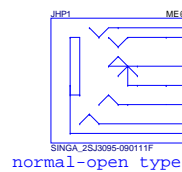
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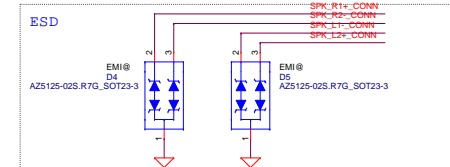
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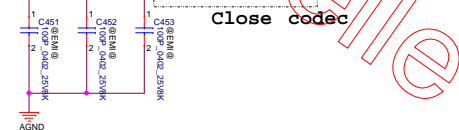
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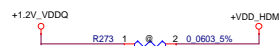
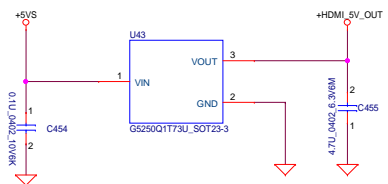
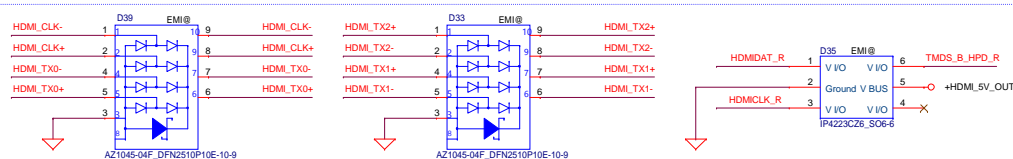
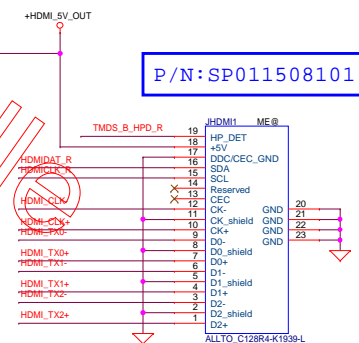
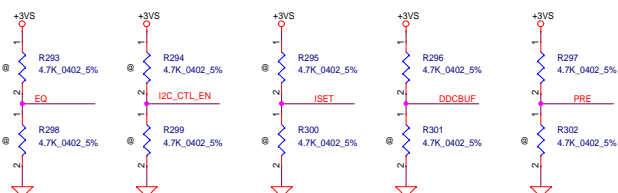
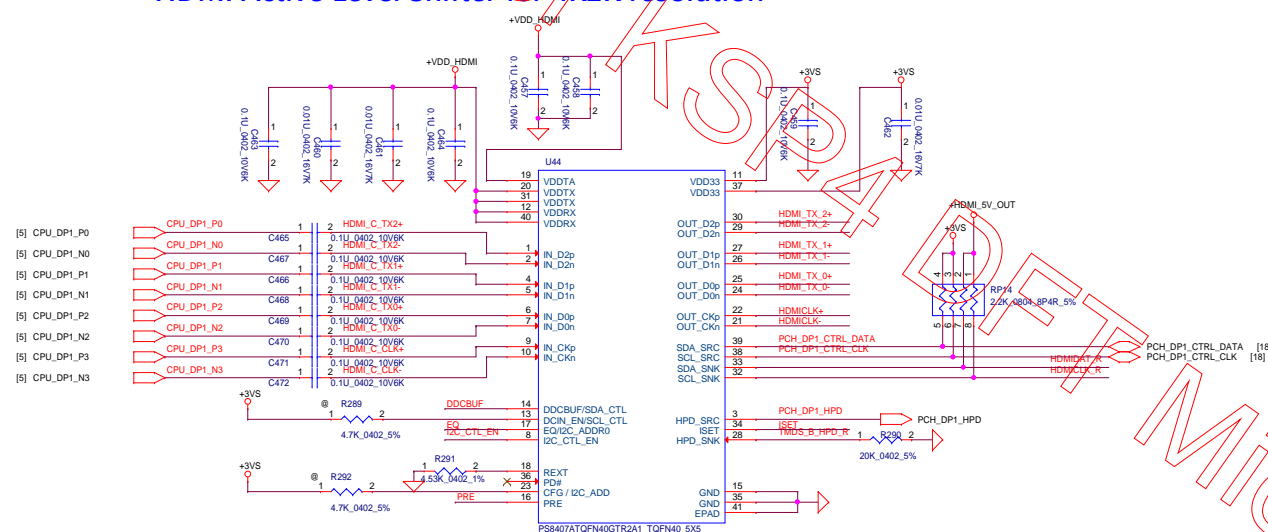


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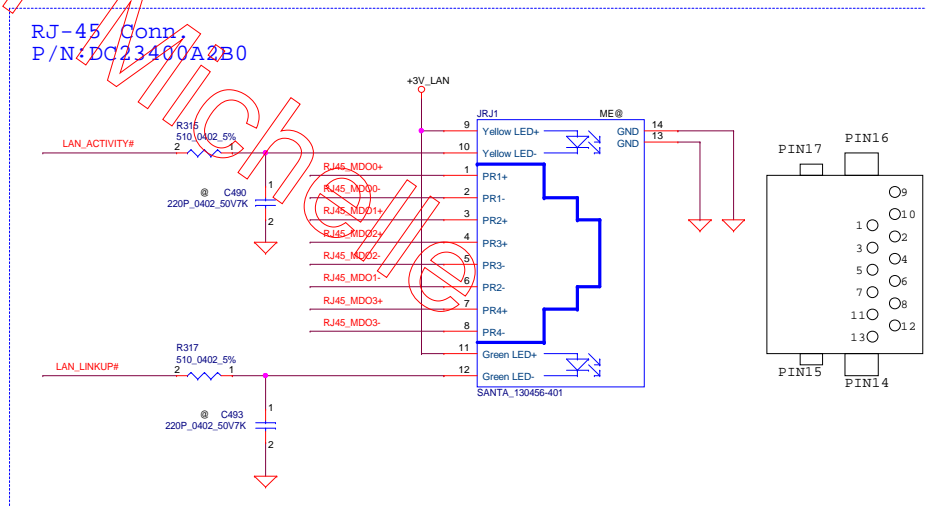
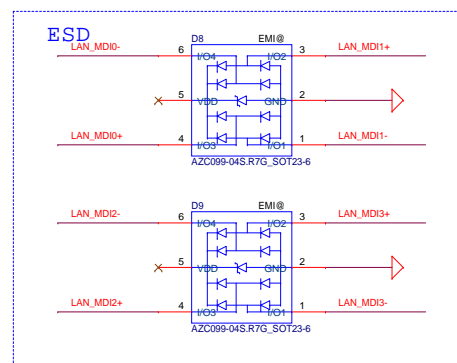
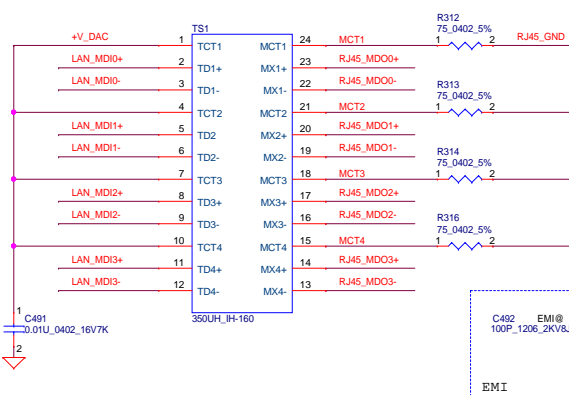
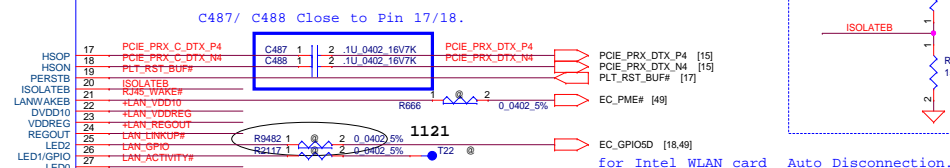
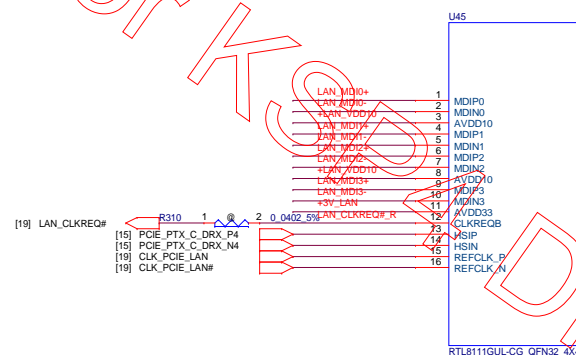
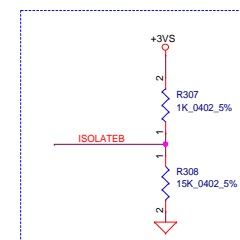
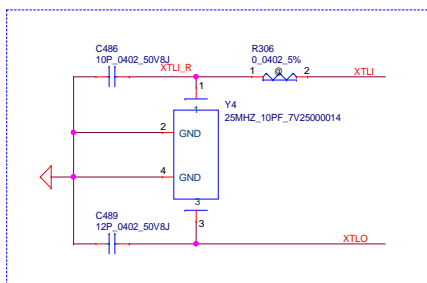
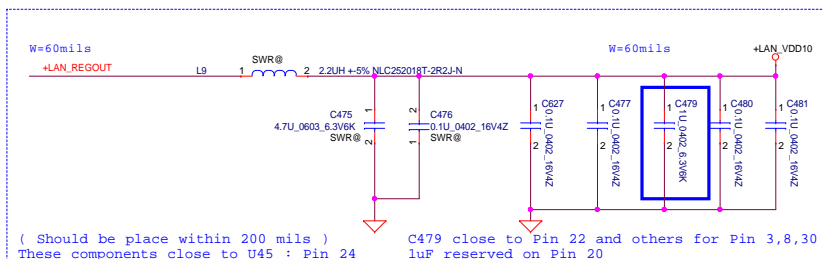
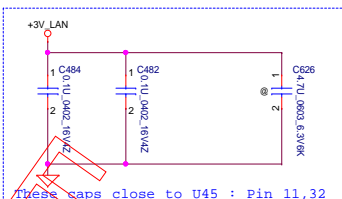
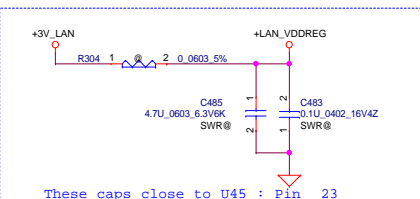
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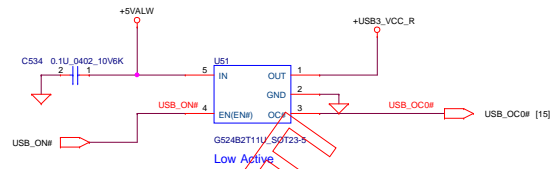
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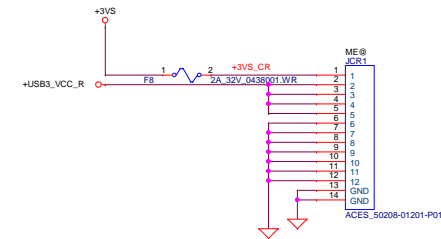
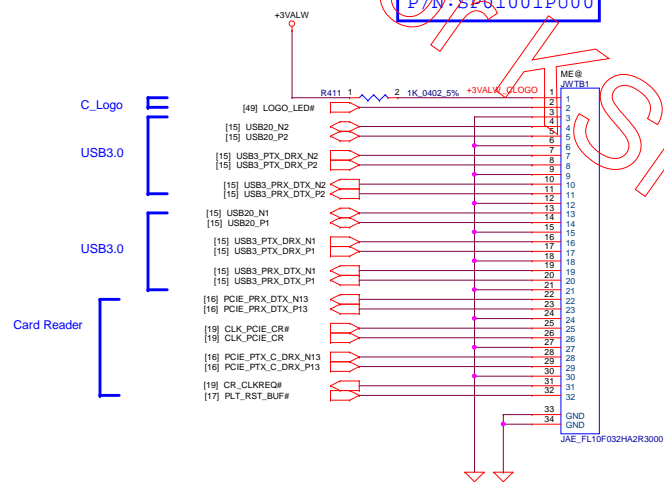
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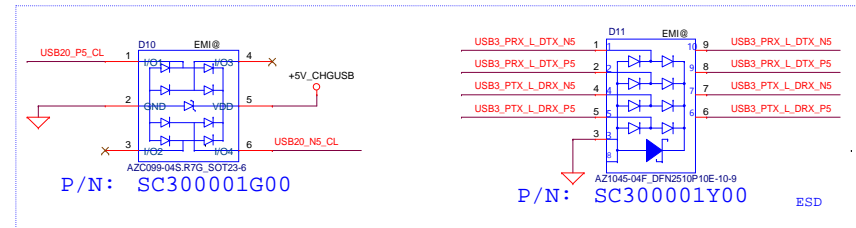
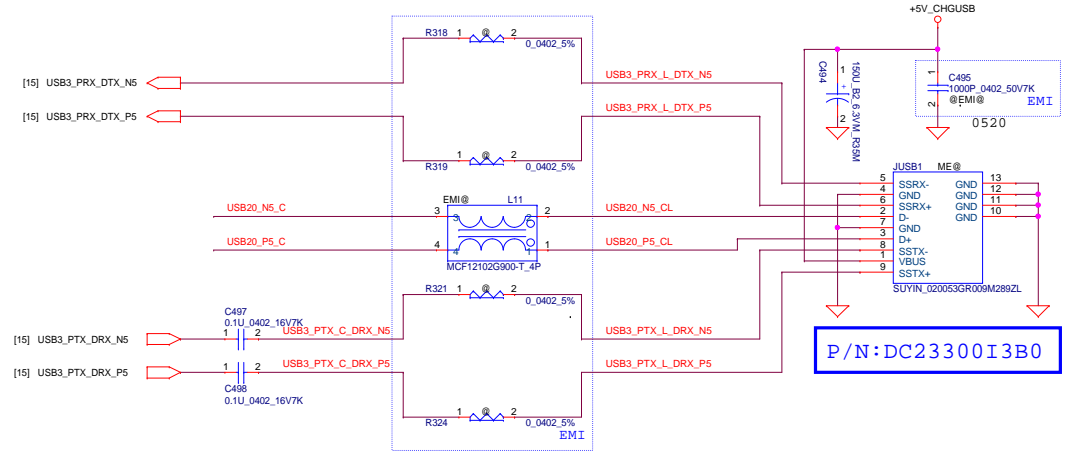
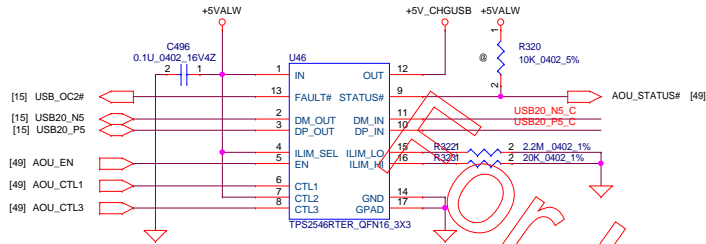
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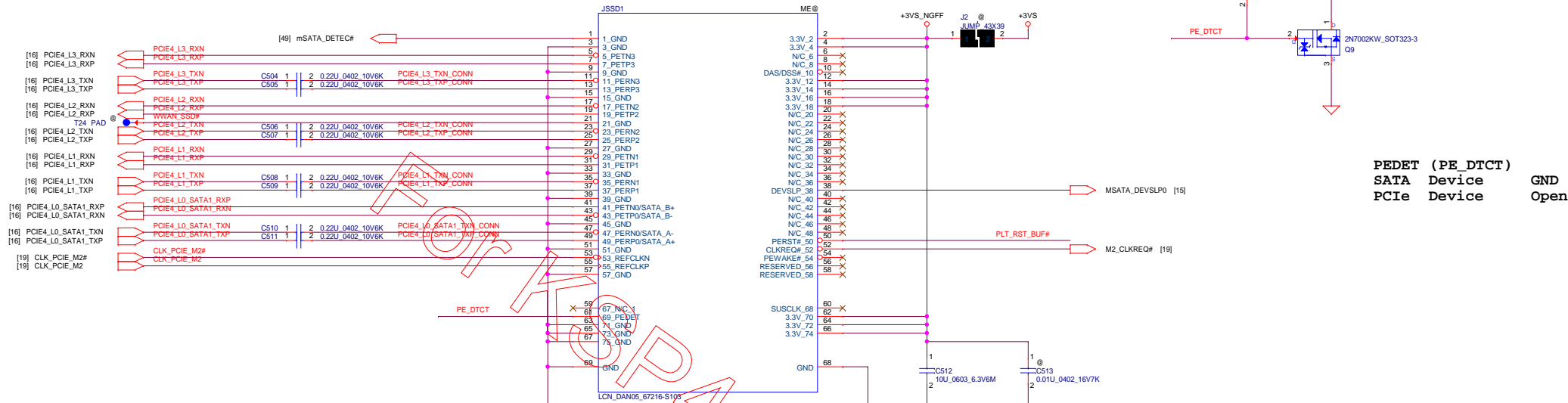
USB30 Left Conn (AOU)

PN: SM070003Y00 x 3

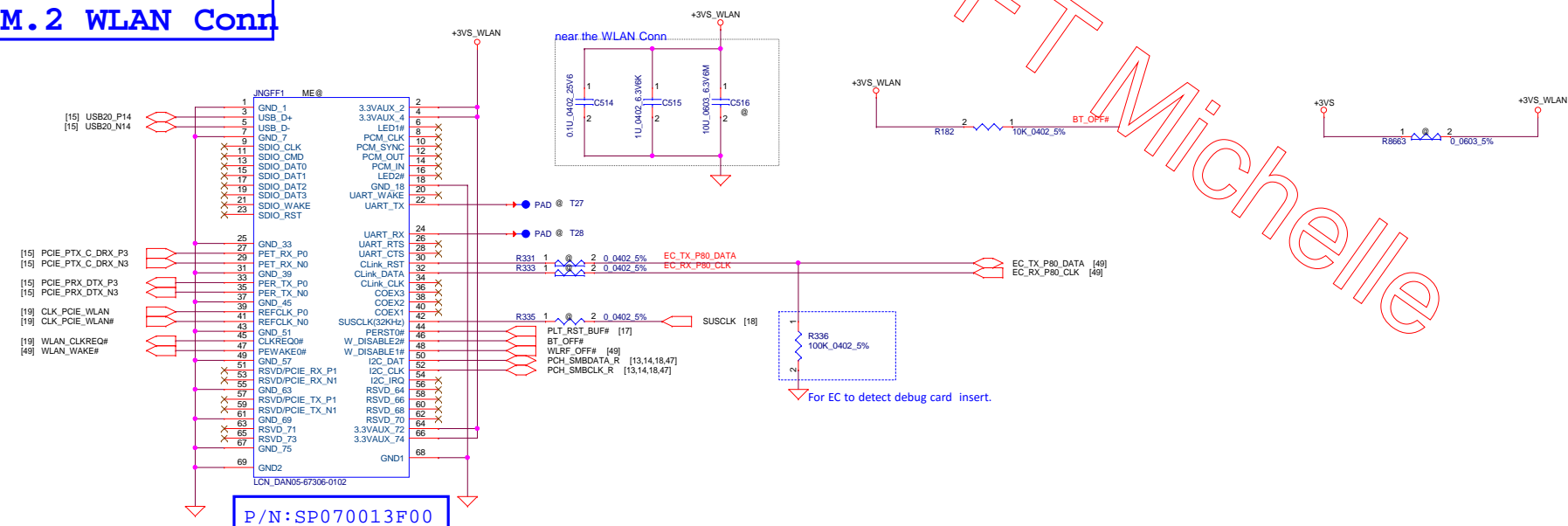


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M.2 mSATA Conn



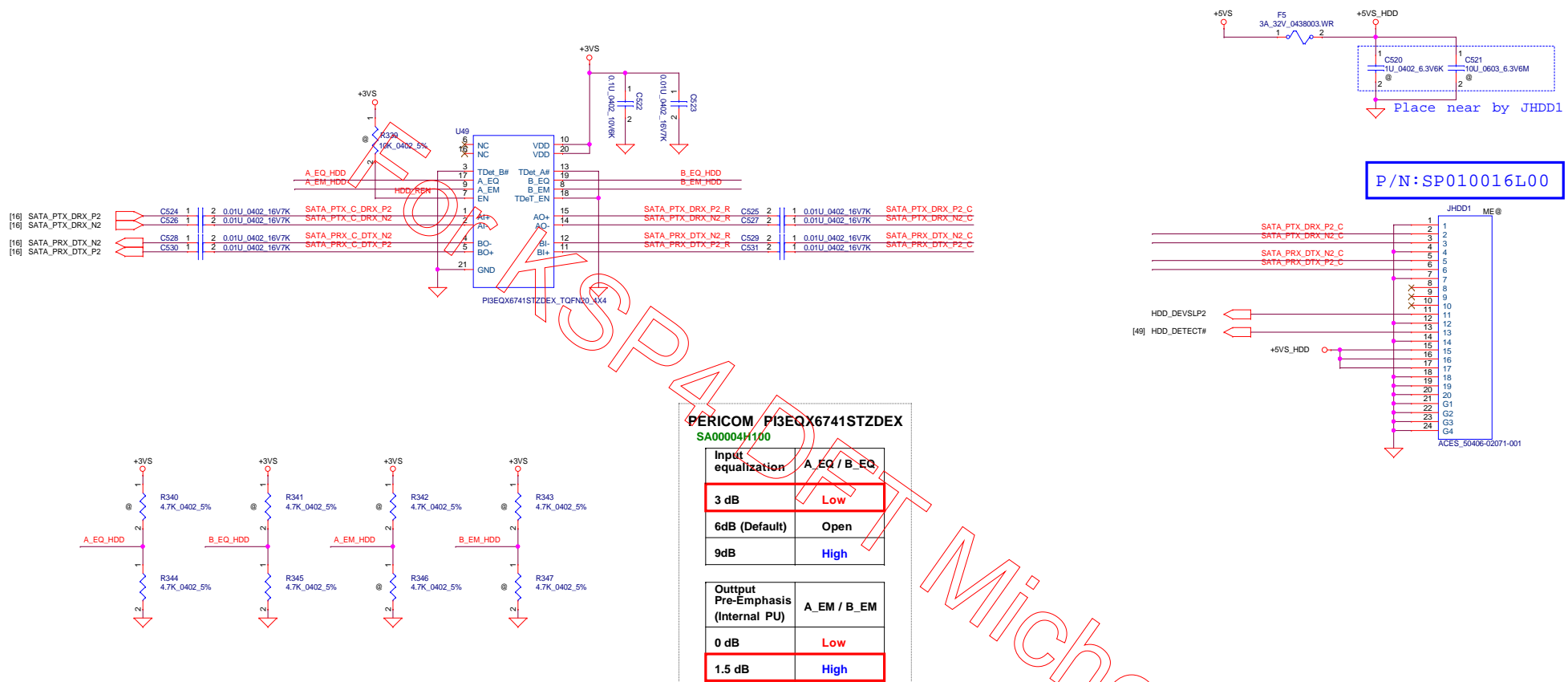
M.2 WLAN Conn



P/N: SP070013F00

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Issued Date	2016/05/13	Deciphered Date	2017/12/31	Title	M.2 WLA/BT/SSD
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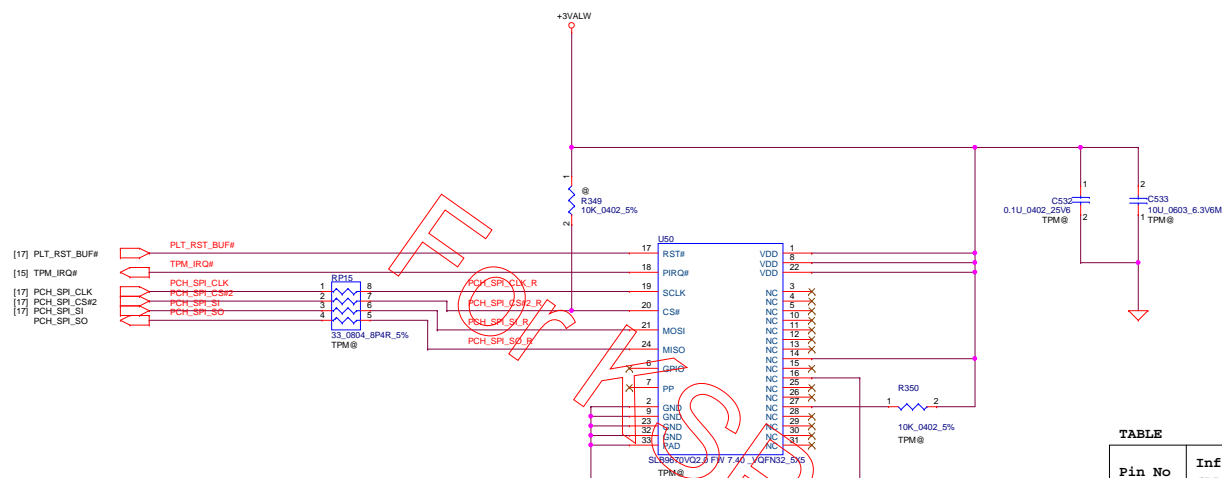
SATA HDD WTB Conn



PERICOM PI3EQX6741STZDEX
SA00004H100

Input equalization	A_EQ / B_EQ
3 dB	Low
6dB (Default)	Open
9dB	High

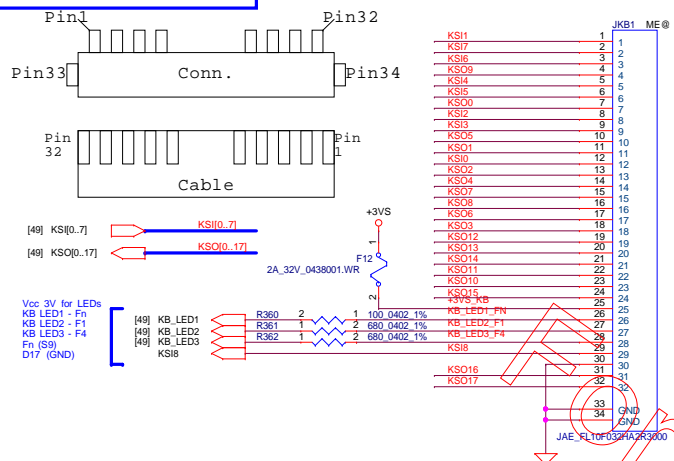
Output Pre-Emphasis (Internal PU)	A_EM / B_EM
0 dB	Low
1.5 dB	High



TABLE

Pin No	Infineon SA00009N200 SLB9670VQ2.0 FW 7.40	ST Micro SA00009SO10 ST33HTPH2E32AHA6
1	VDD	NC
2	GND	GND
3	NC	NC
4	NC	NC
5	NC	NC
6	GPIO	NC
7	PP	PP
8	VDD	NC
9	GND	NC
10	NC	NC
11	NC	NC
12	NC	NC
13	NC	NC
14	NC	NC
15	NC	NC
16	NC	NC
17	RST#	SPI_RST#
18	PIRQ#	SPI_PIRQ#
19	SCLK	SPI_CLK
20	CS#	SPI_CS#
21	MOSI	MOSI
22	VDD	VPS
23	GND	NC
24	MISO	MISO
25	NC	NC
26	NC	NC
27	NC	NC
28	NC	NC
29	NC	NC
30	NC	NC
31	NC	NC
32	GND	NC

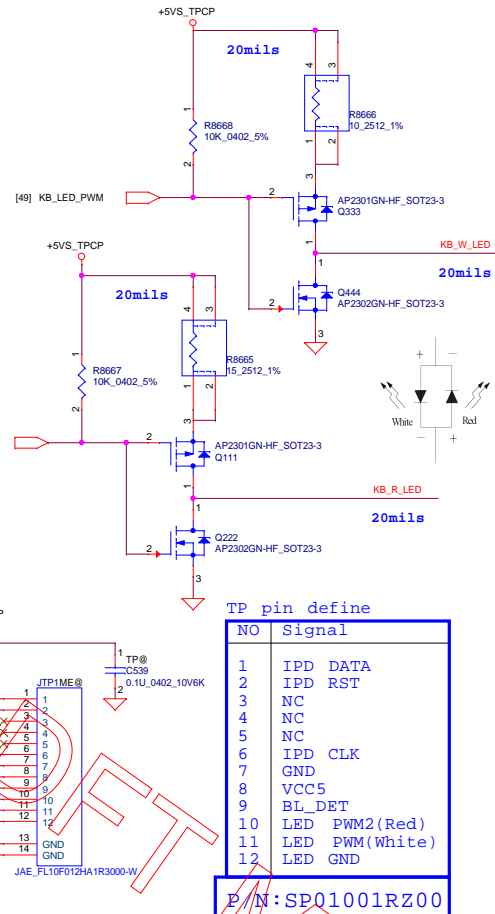
Int KB Conn



P/N:SP01001PU00

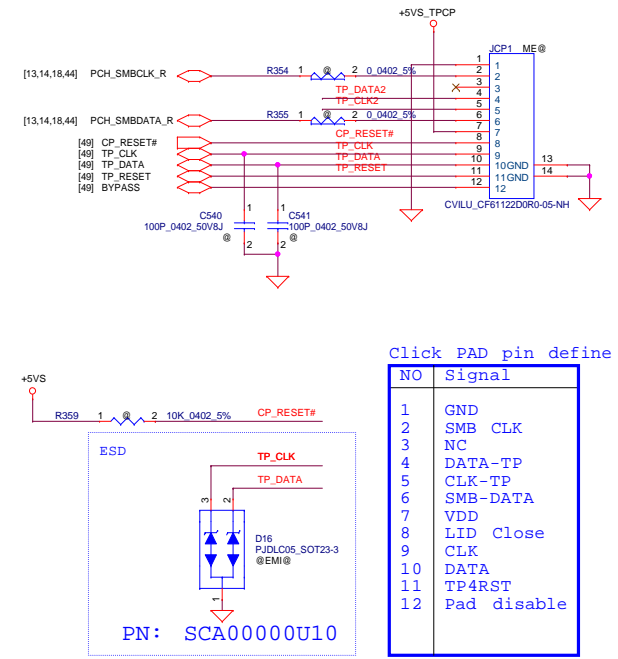
Track Point

KB_LED_PWM OD	KB_LED_PWM2 OD	White	Red
5 V	0 V	OFF	ON
0 V	5 V	ON	OFF
5 V	5 V	OFF	OFF
0 V	0 V	NA	NA



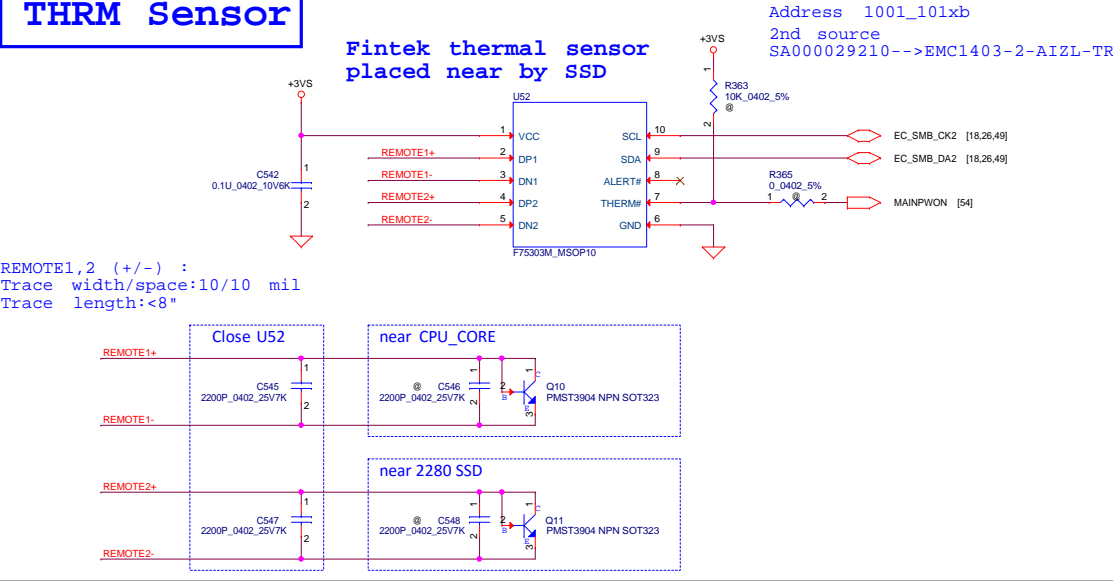
Click PAD

PN:SP010025L00



THRM Sensor

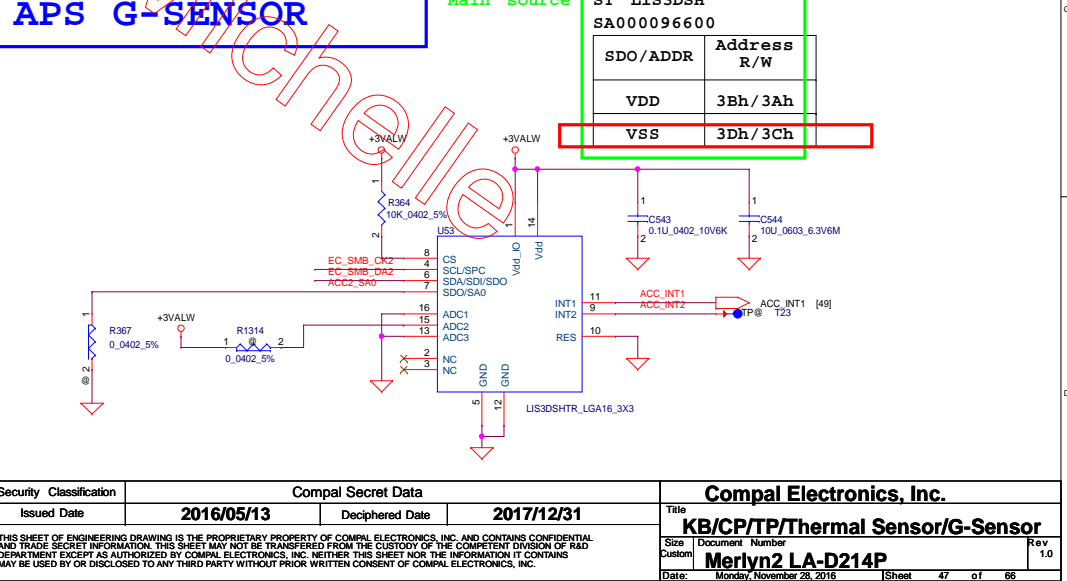
Fintek thermal sensor
placed near by SSD



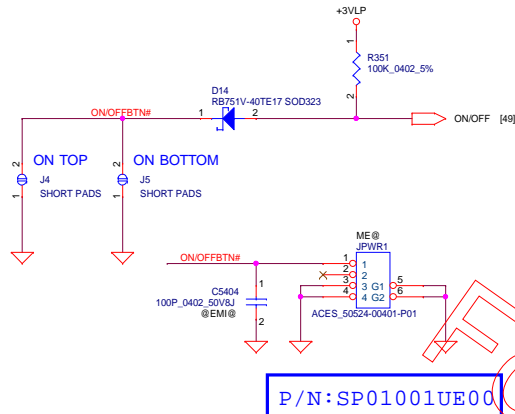
APS G-SENSOR

Main source

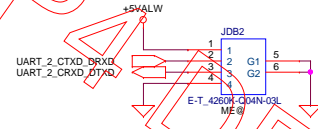
ST LIS3DSH	
SA000096600	
SDO/ADDR	Address R/W
VDD	3Bh/3Ah
VSS	3Dh/3Ch



PWRBTN Conn

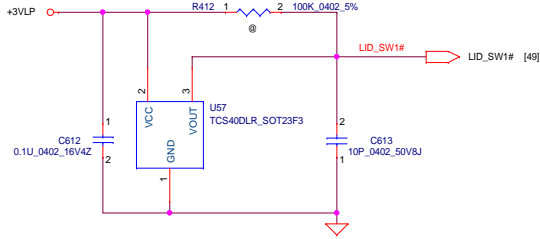


Debug Conn



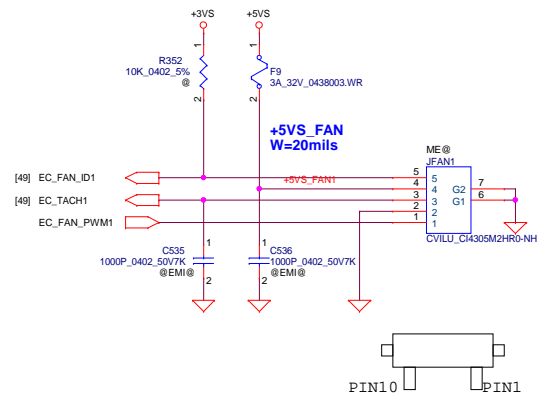
WIN 7 Debug conn

Hall Sensor



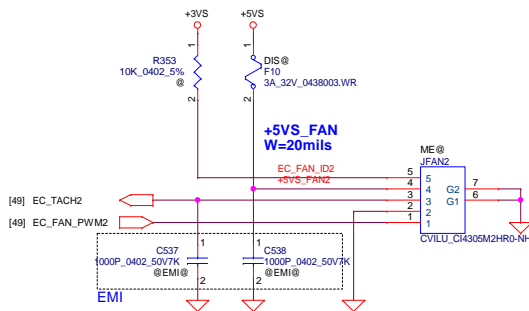
CPU FAN Conn

P/N: SP020016N00



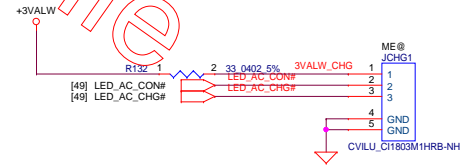
dGPU FAN Conn

P/N: SP020016N00



AC CHG Conn

P/N: SP01001KF10



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				Rev	1.0

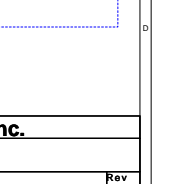
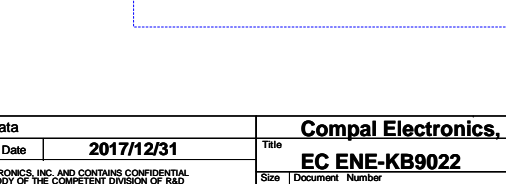
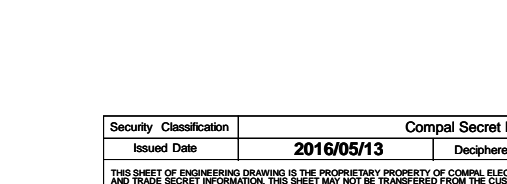
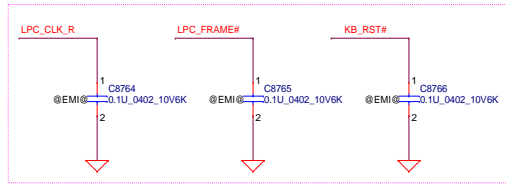
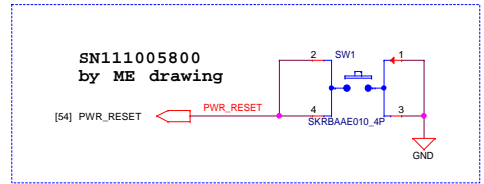
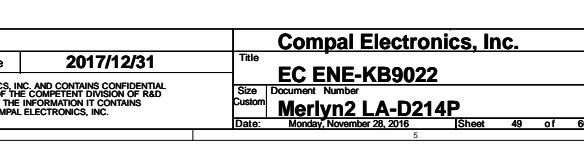
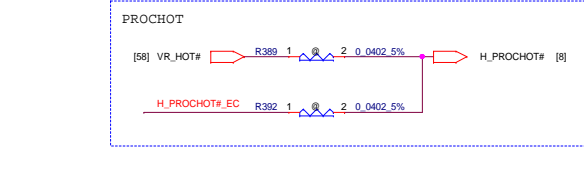
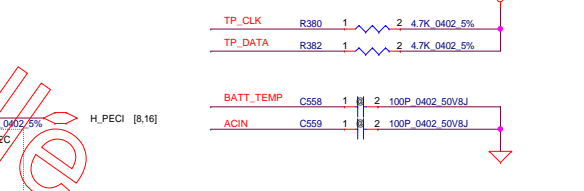
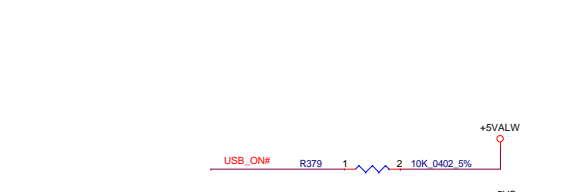
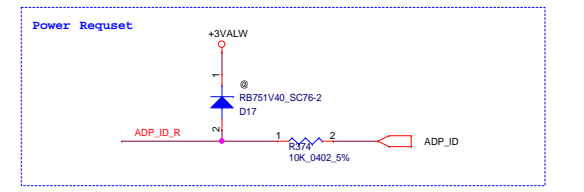
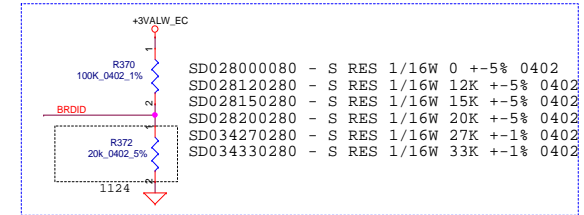
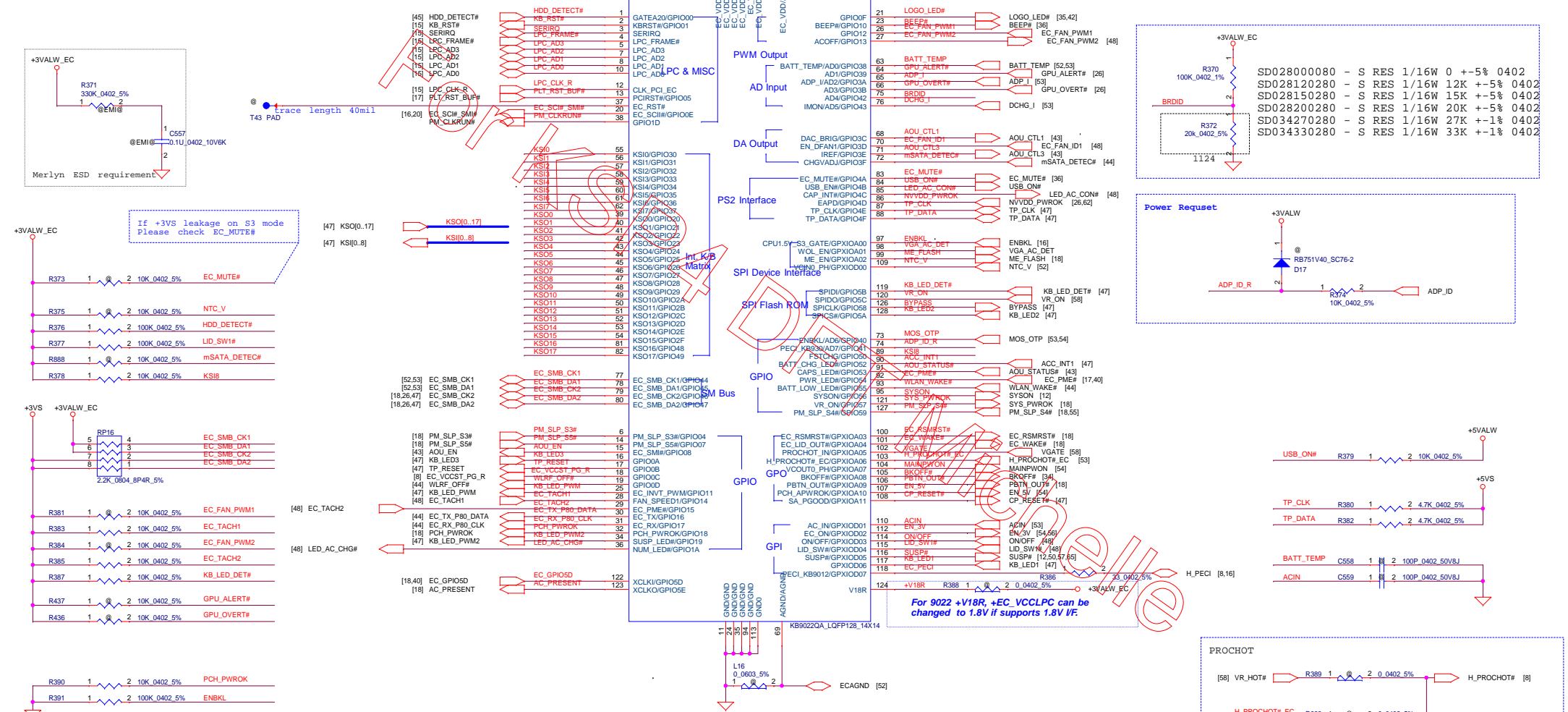
EC KB9022

KB9022 A v.02

GPIO W/O internal-PH:

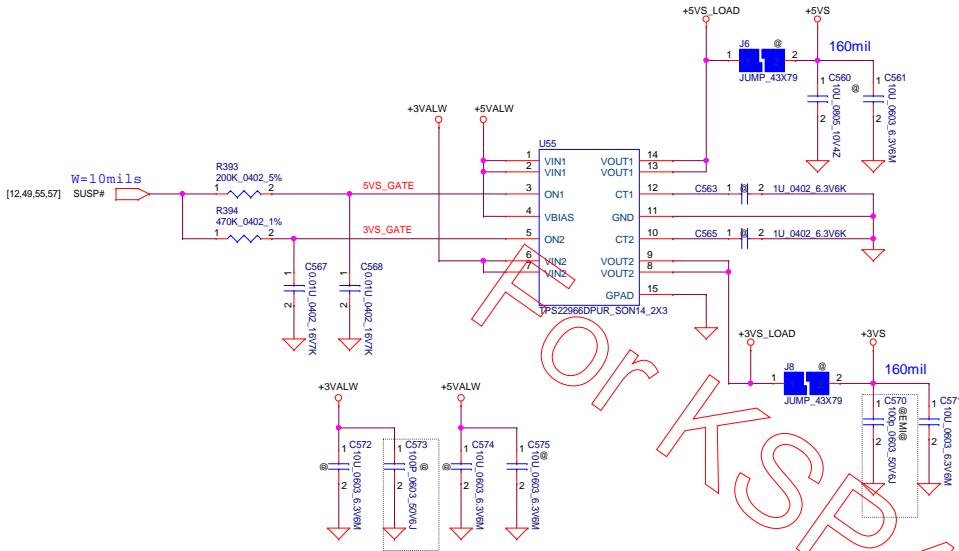
- | | |
|-----------|------------|
| 1. GPIO44 | 6. GPIO4B |
| 2. GPIO45 | 7. GPIO4E |
| 3. GPIO46 | 8. GPIO4F |
| 4. GPIO47 | 9. GPIO50 |
| 5. GPIO4A | 10. GPIO51 |

Vcc 3.3V +/- 5%		R370 100K +/- 1%			
Board ID	R372	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD
SDV	0K +/- 5%		0.000V	0.300V	0x00 - 0x0B
FVT	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
SIT	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
SVT	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
TBD	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
TBD	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
TBD	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54

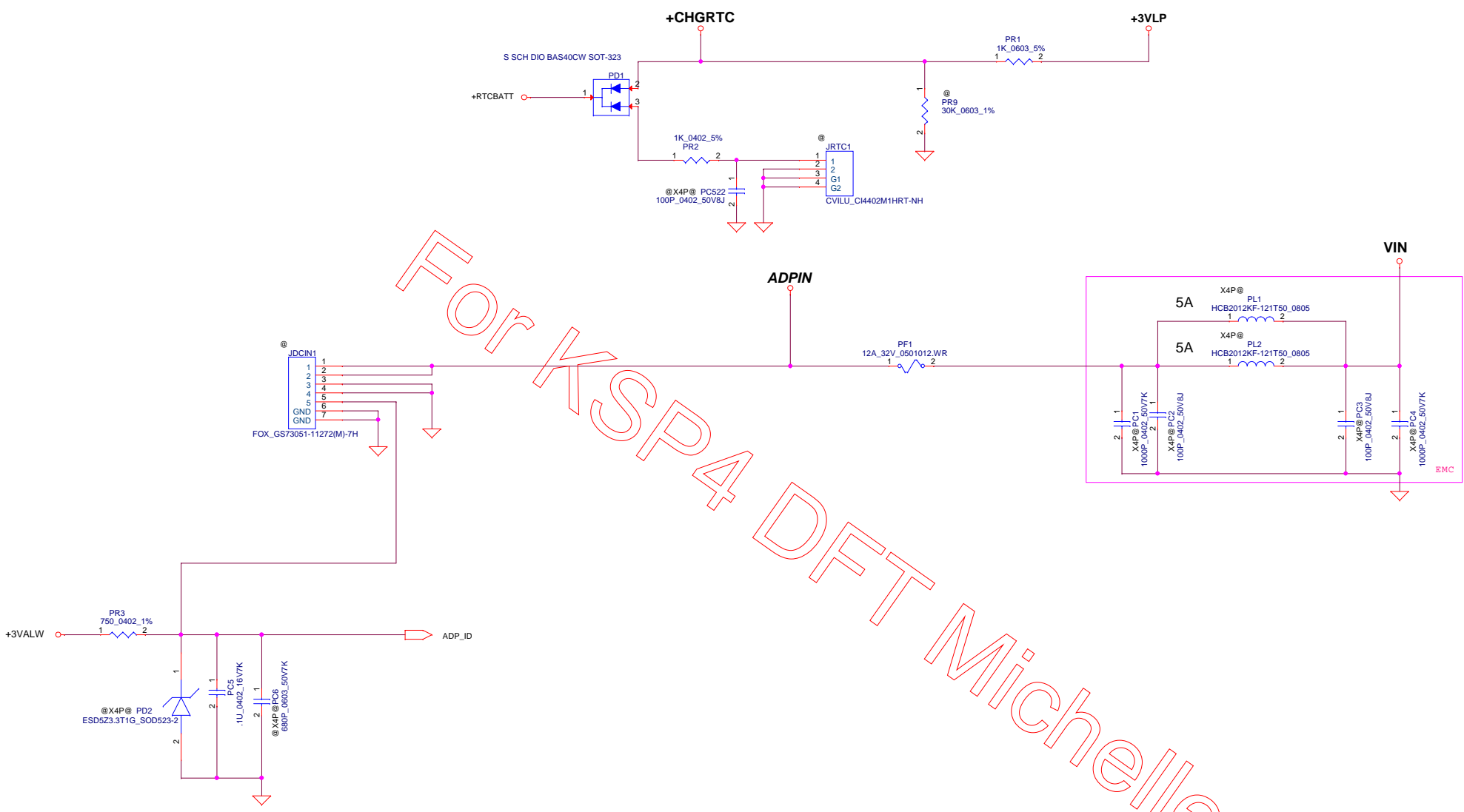


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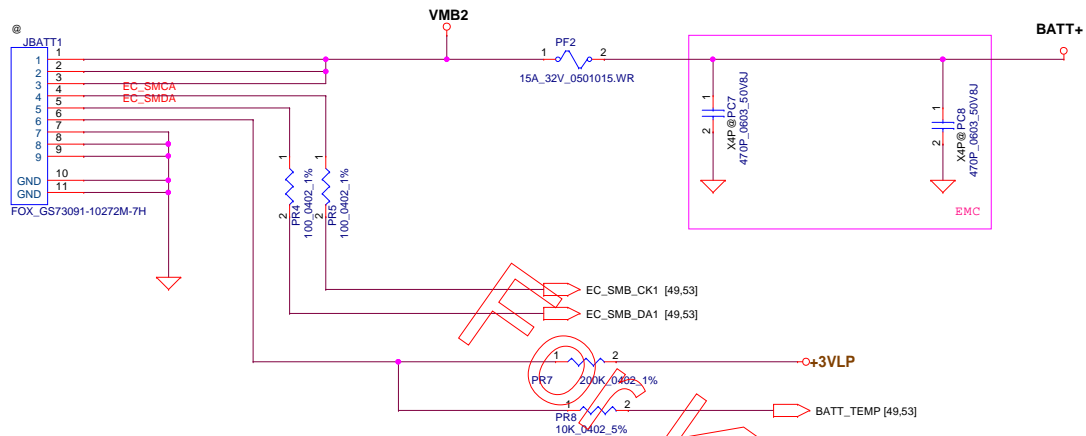
+5VALW TO +5VS
+3VALW TO +3VS



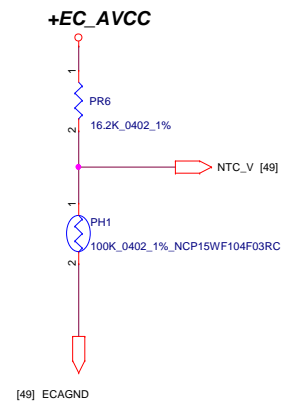
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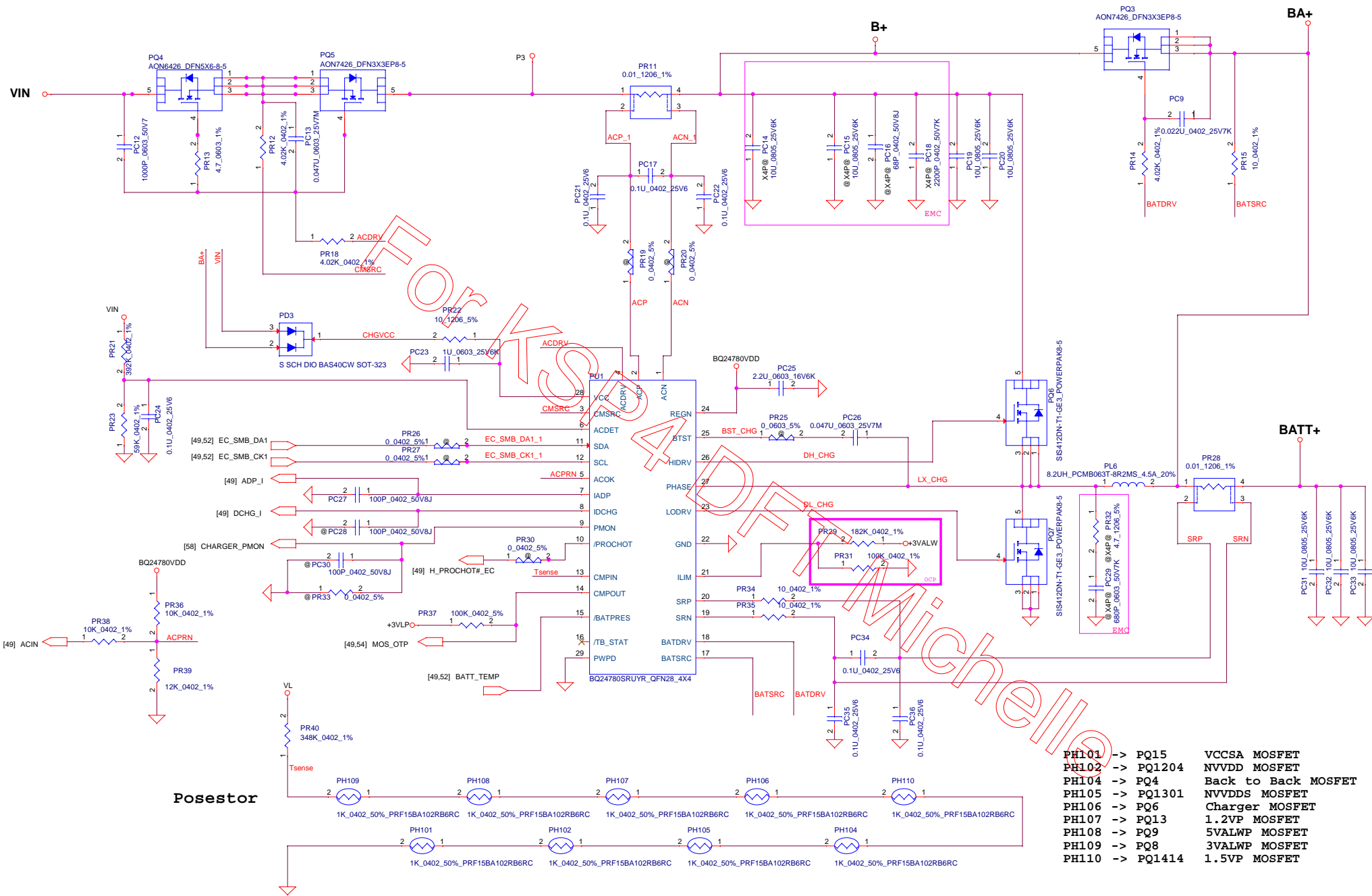


PH1 under CPU bottom side :
CPU thermal protection at 93 degree C



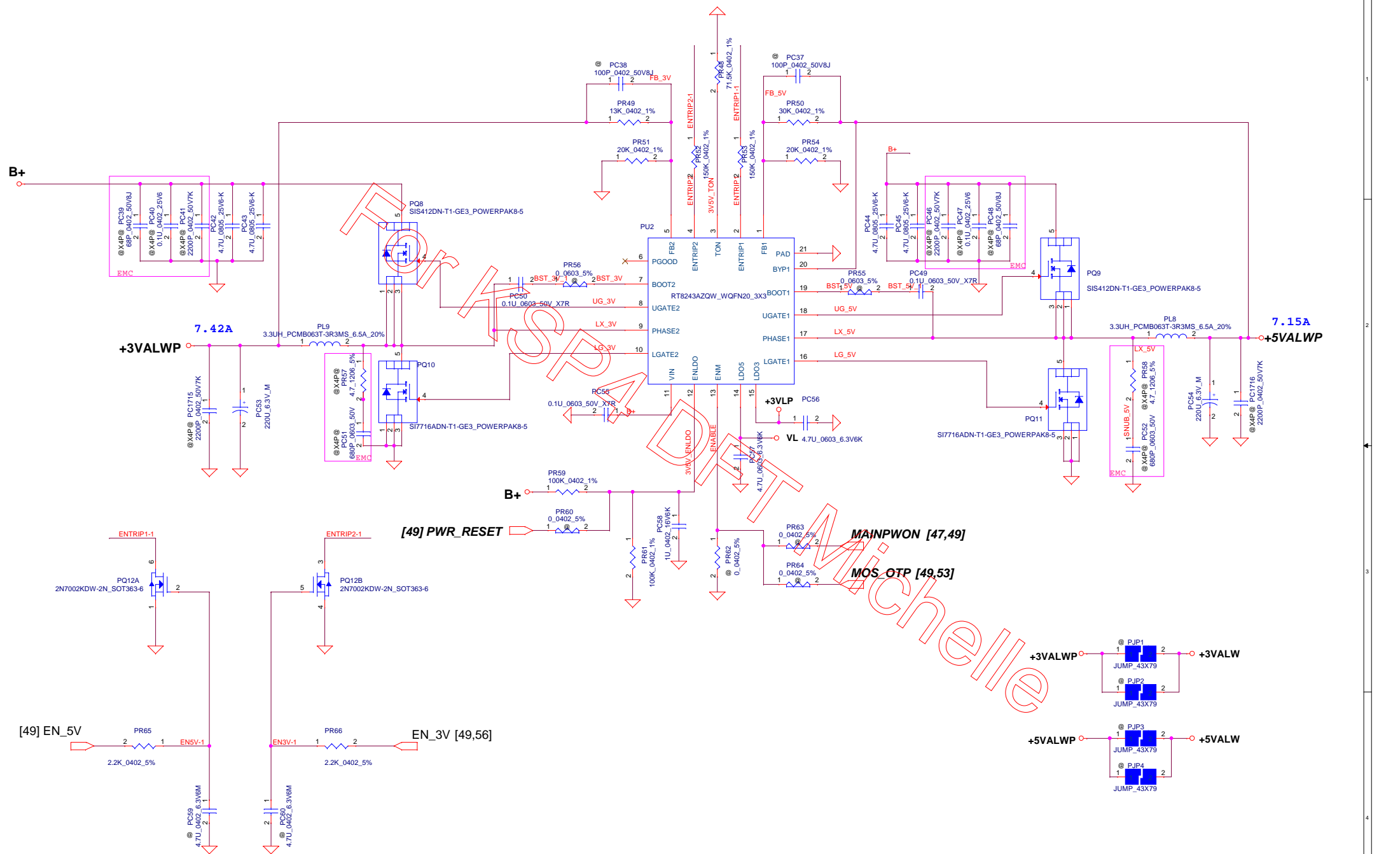
PH1 :	Temp .	Rman .	Rnor .	Rmin . (Kohm)
	93	7.3419	7.0792	6.8253

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2017/12/31				Title				PWR-BATTERY CONN/OTP			
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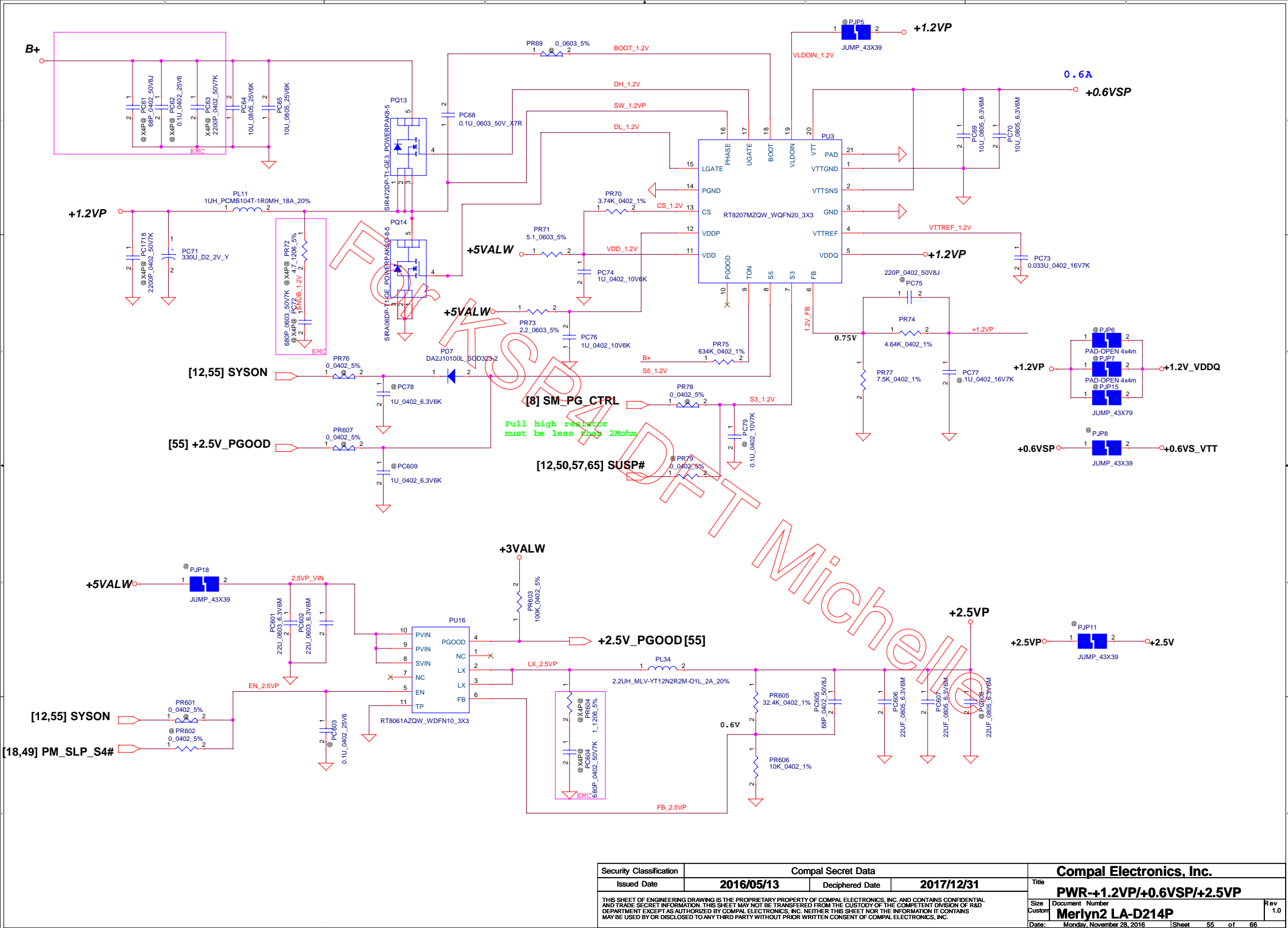


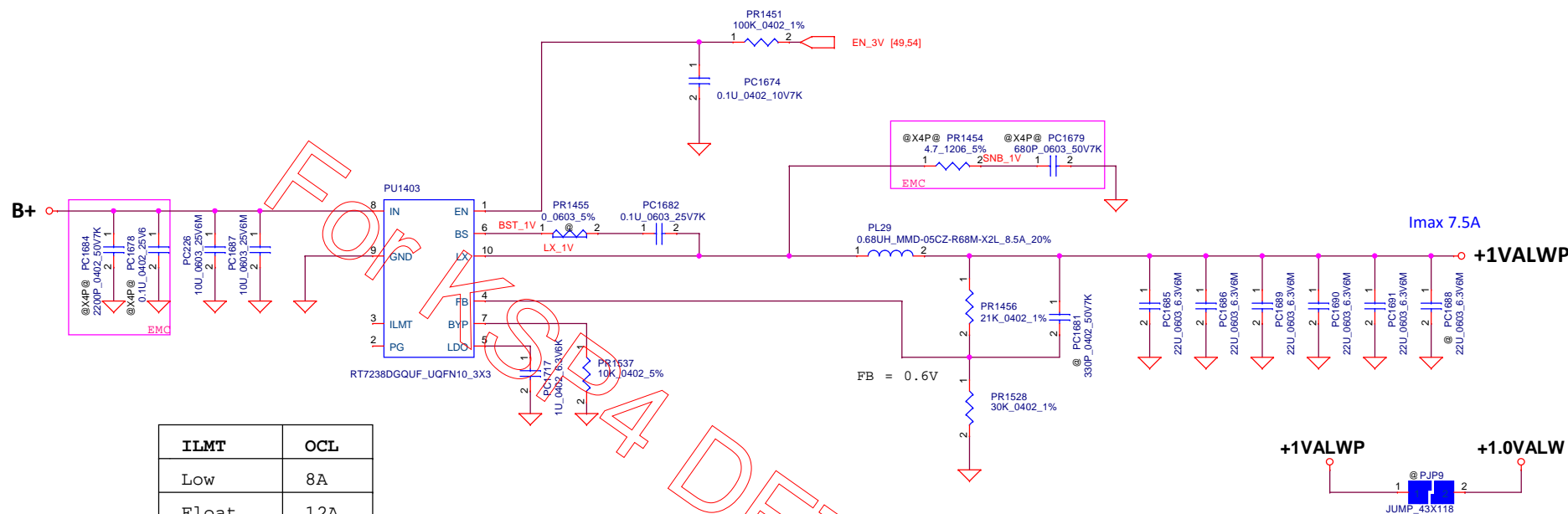
- PH101 -> PQ15 VCCSA MOSFET
- PH102 -> PQ1204 NVVDD MOSFET
- PH104 -> PQ4 Back to Back MOSFET
- PH105 -> PQ1301 NVVDDS MOSFET
- PH106 -> PQ6 Charger MOSFET
- PH107 -> PQ13 1.2VP MOSFET
- PH108 -> PQ9 5VALWP MOSFET
- PH109 -> PQ8 3VALWP MOSFET
- PH110 -> PQ1414 1.5VP MOSFET

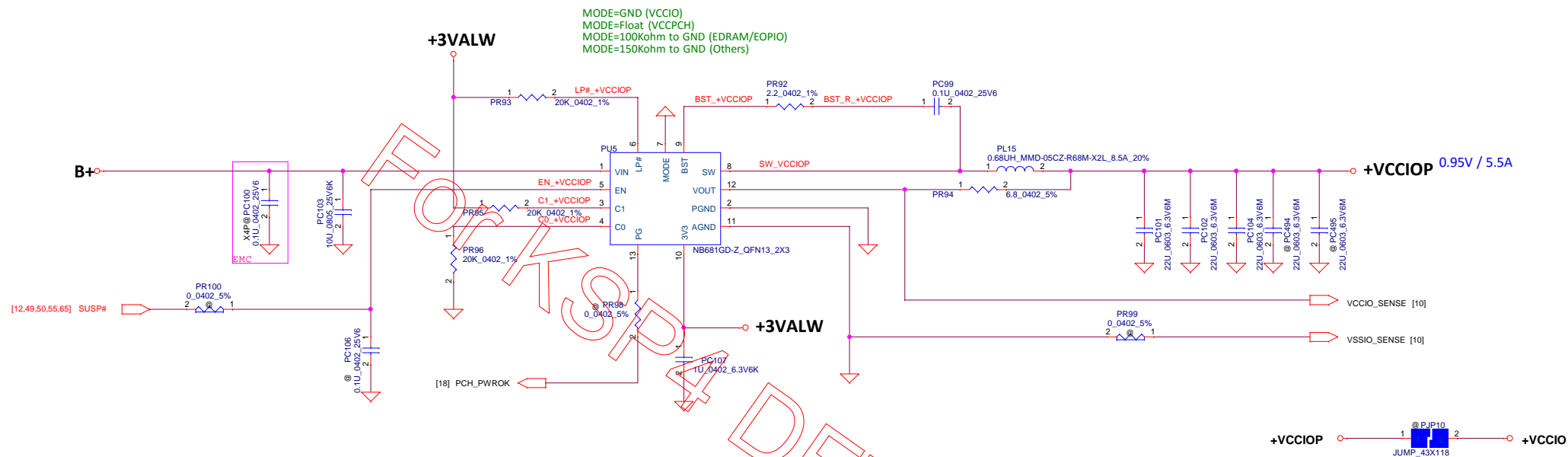
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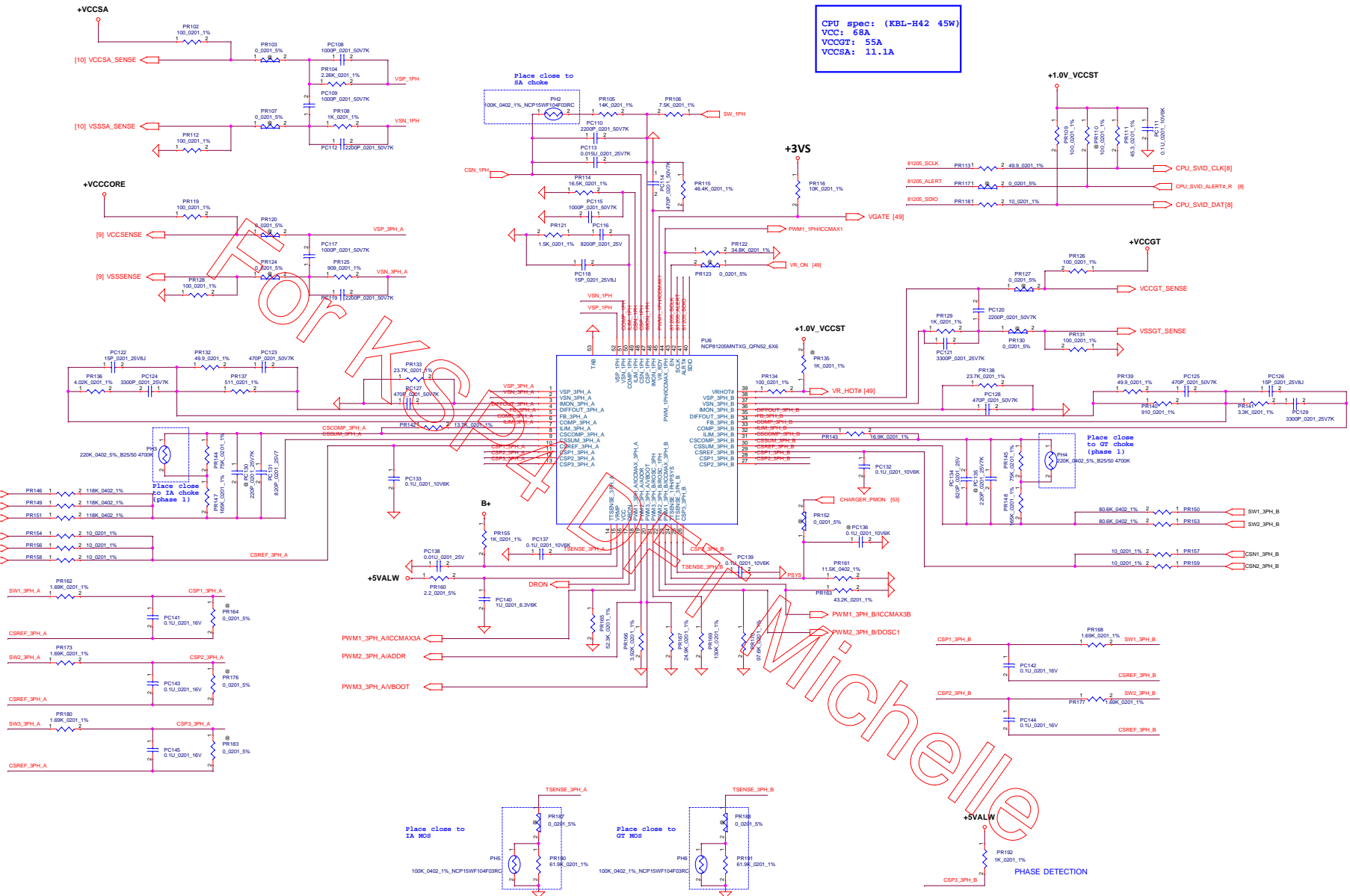


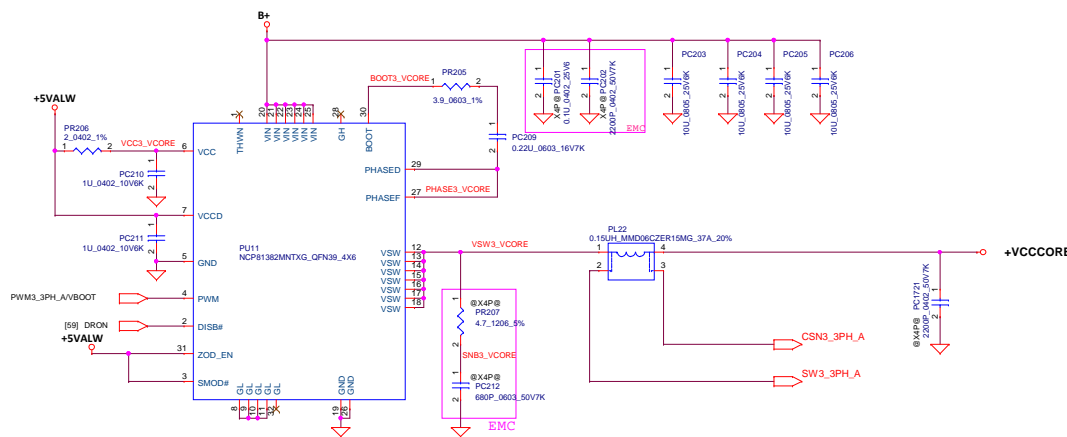
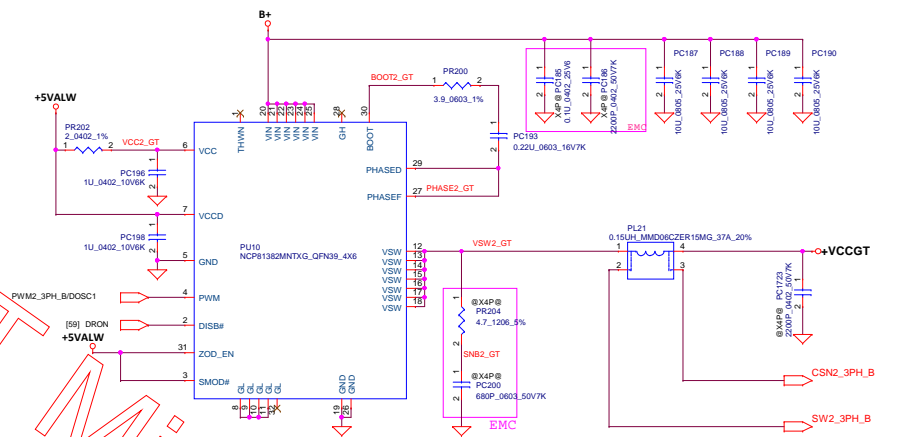
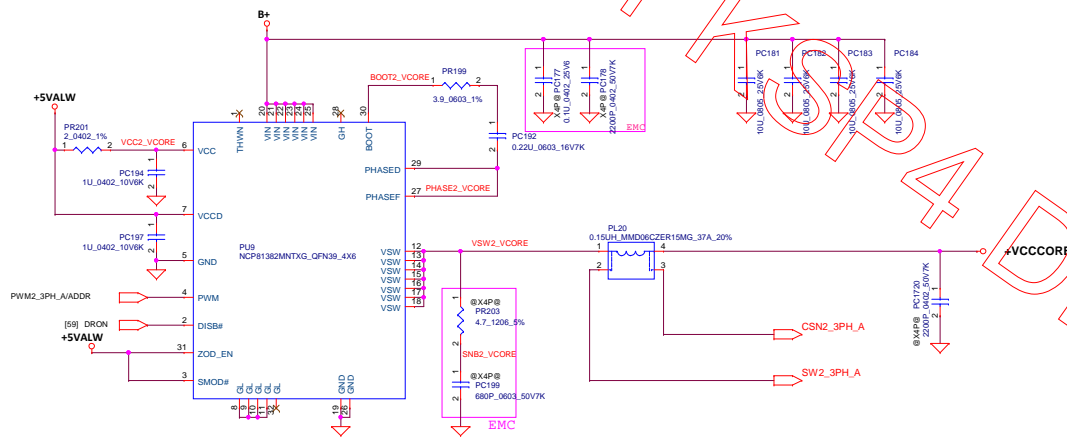
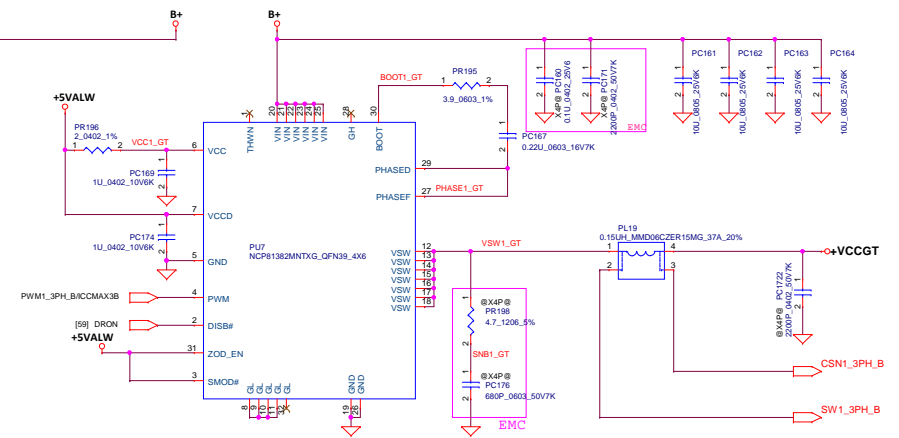
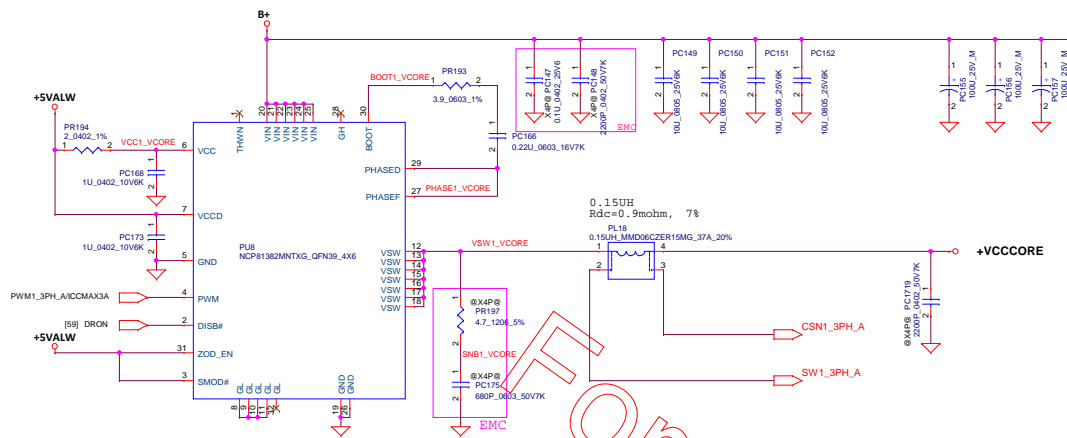
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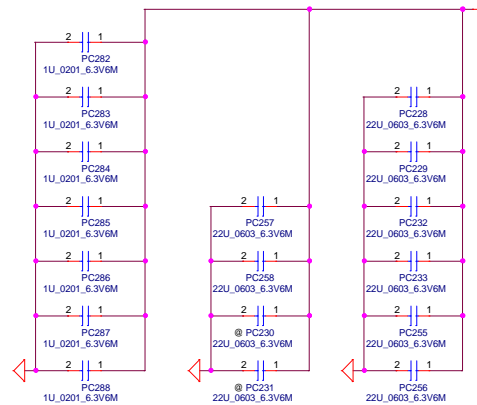
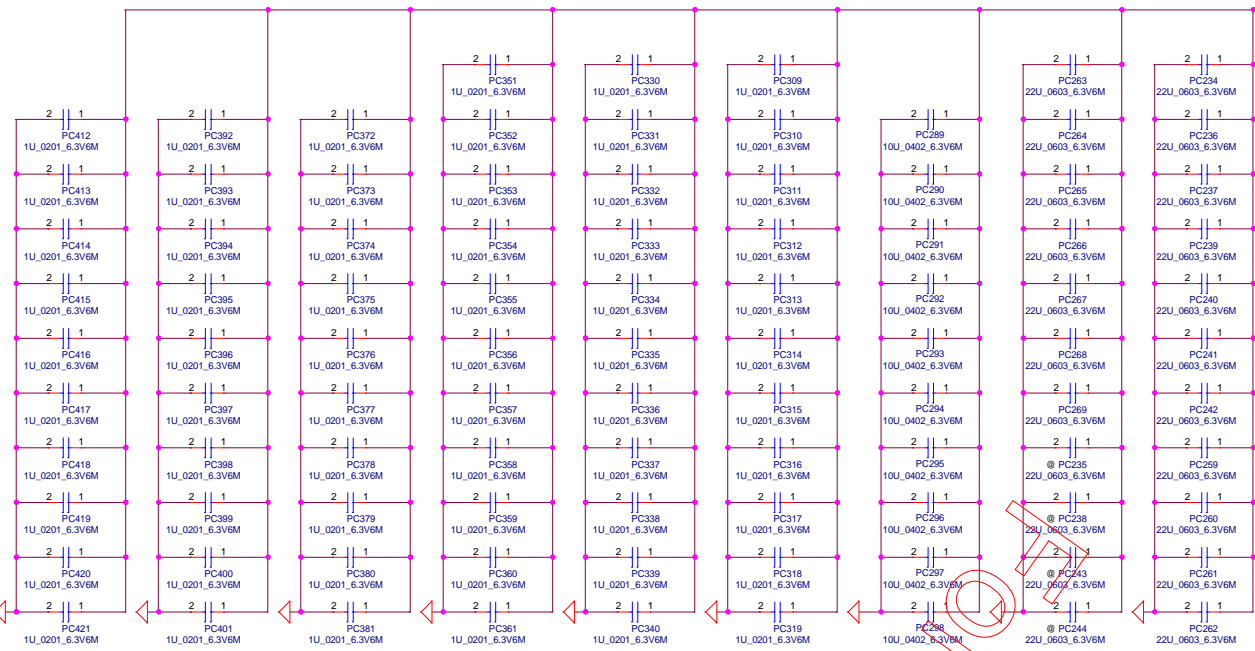
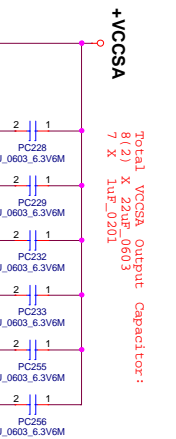
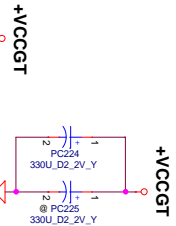
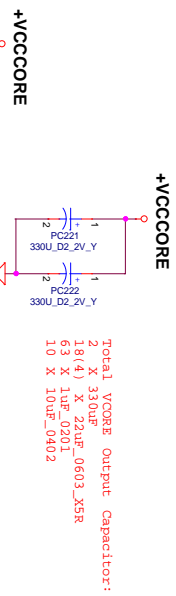






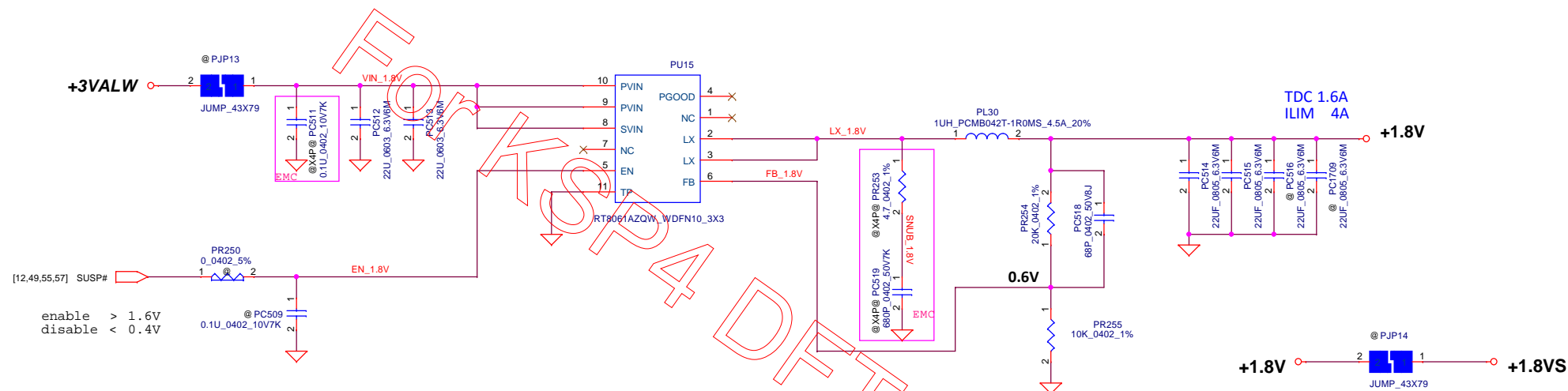


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				PWR-VCCCORE/VCCGT	
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Michelle

Security Classification			Compal Secret Data			Title		
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Version change list (P.I.R. List)

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for EE

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

For KSP4 DFT Michelle

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